Design and Performance Analysis of Low Power ALU

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Abstract
In this paper, the gate level circuit of a 1-bit CMOS Arithmetic and Logic Unit (ALU) is designed and performance is analyzed. The main requirement of any technology is to design and develop low power circuit. Along with the power, high speed ICs are leading the VLSI industry. Here the performance of the proposed design is simulated and evaluated in terms of delay and power using tanner tools S-EDIT with different FANIN's using NAND gate. Power and delay has a major impact while designing any circuit. So, these factors play a major role in deciding the efficiency of the designed circuit.

Keywords
CMOS, NAND, NOR, ALU, FANIN

I. Introduction

Digital circuits consist of logic gates implemented in the Complementary Metal Oxide Semiconductor (CMOS) technology. The power consumption of these circuits has two components. The dynamic power is consumed only when the circuit performs a function and signals change. Leakage or static power is consumed all the time, i.e., even when the circuit is idle. The dynamic power cannot be eliminated completely because it is caused by the computing activity. It can, however, be reduced by circuit design techniques. Whenever a logic gate changes state, power is consumed. The solution is then realized at the transistor level designs. In this work, a 1-bit ALU is designed at transistor level for low power and minimum area. The rest of the paper is organized as follows; Section II will discuss about the ALU. Section III will discuss for the design of ALU cell. Followed by ALU designs, Simulation results and conclusion.

II. ALU

In computing, an Arithmetic and Logic Unit (ALU) is a digital circuit that performs integer arithmetic and logical operations. The ALU is a basic block of the central processing unit of a computer, and even the simplest microprocessors that has a work of maintaining the timers. The processors accommodate very powerful and very complex ALUs inside modern CPUs and Graphics Processing Units (GPUs), a single component may contain a number of ALUs. Two important performance parameters of all digital circuits, for most applications are maximizing speed and minimizing power consumption. In this work, a 1-bit ALU is designed at transistor level for low power and minimum area. As per the analysis the power consumption is minimum with the channel length of 45 nm compared with the channel length of 90 nm.

Fig. 1 shows the basic block diagram of ALU. These blocks are designed in such a way that all the arithmetic and logic operations are performed with accuracy in less area, delay and power. To decrease the size of this macro circuit, FAN-IN concept is used. A universal gate can implement any Boolean function without using any other gate. So, NAND gate realization of ALU is discussed here.

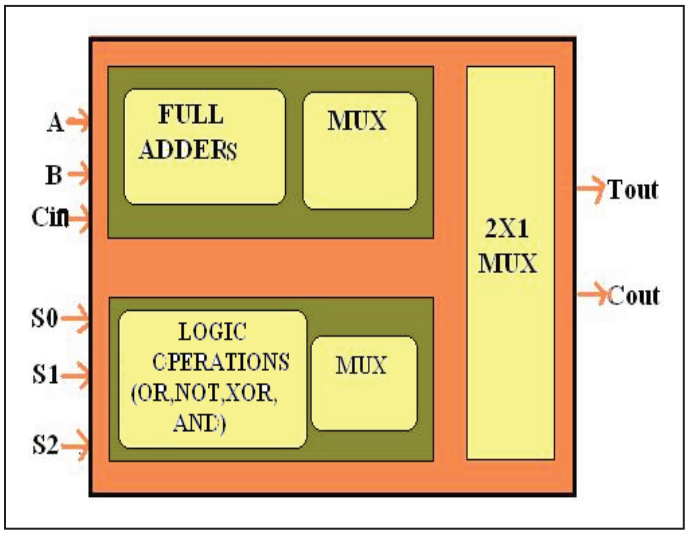


Fig. 1: Block Diagram of ALU

A. Fan-In

Fan-in is the number of inputs a logic gate can handle. Using logic gates with higher fan-in will help reducing the depth of a logic circuit. If number of input exceeds, the output will be undefined or incorrect. So we have restricted up to 4 inputs only. Fig. 2 shows NAND GATE with different FAN IN 2, 3 and 4.

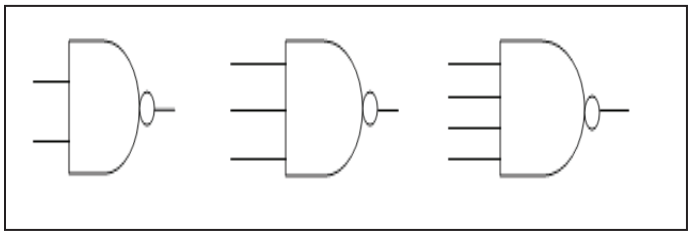


Fig. 2: NAND GATE with FAN IN 2, 3 and 4.

III. Proposed Design

A. Design of a 1-bit ALU

ALU which is a important element in central processing unit consists of arithmetic and logic units. These two basic units are comprised together using a summing unit. The main component for arithmetic unit is parallel adder, which consists of a number of full adders connected in cascade connection. The different types of operations can be obtained by this unit by changing the inputs to the parallel adder. Fig. 4 shows the arithmetic operations obtained when one of the two inputs is changed. Here A and B are two inputs of parallel adder, where B is changed and A remains the same.

The parallel adder inputs may be of any number of bits in value. The input carry C_{in} given to the full adder circuit in the least significant bit position and the C_{out} comes from the full adder circuit in the most significant bit position. From the fig. 3(a) to 3(h) various types of eight operations are achieved by changing the B input and C_{in}. So to design the circuit we need two parts, one is control circuit and another one is full adder.

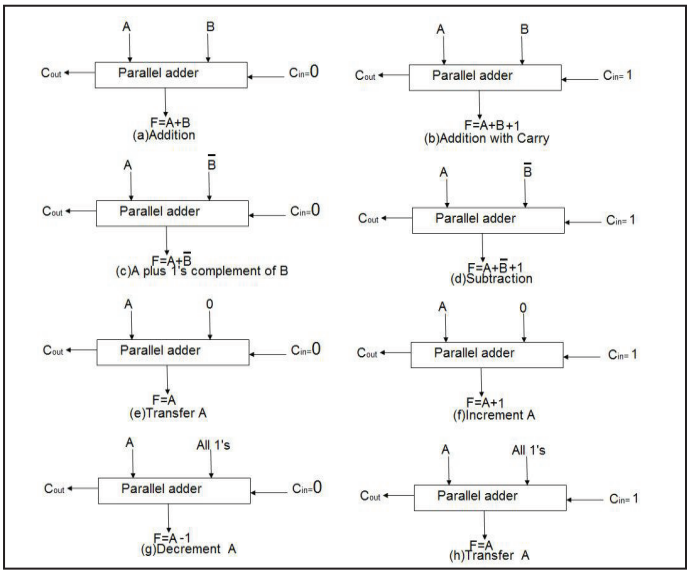


Fig. 3: Eight Operations Obtained when one of the Two Inputs is Changed

The basic logic diagram of a 4 bit arithmetic circuit is shown in fig. 4. This circuit controls the input B to provide various type of operation shown in fig. 4 and consists of two NAND gates, one OR gate and one NOT gate. S_1 and S_0 is two selection lines used to control the B input. When $S_1 S_0 = 00$ the output of the OR gate Y=0, When $S_1S_0 = 01$ the output of the OR gate Y=B, When $S_1S_0=10$ the output of the OR gate Y=B', When $S_1S_0=11$ the output of the OR gate Y=B+B'=1. This parallel adder constitutes of four full adders. The carry into the first stage is the input carry. The carry out of the fourth stage is the output carry. The selection variables are S_1, S_0 and C_{in}. Variables S_1S_0 control all the B inputs to the full adder circuits. The A inputs go directly to the other inputs of the full adder section multiplexers plays an important role. A 4:1 Mux is used in the logic section. In the logic unit various operations like signed shifts (arithmetic left shift and the arithmetic right shift), logical shifts (logical left shift and the logical right shift), circular shift s (circular left shift and the circular right shift) etc., are performed. With the help of selection lines one of the logic operations is performed.

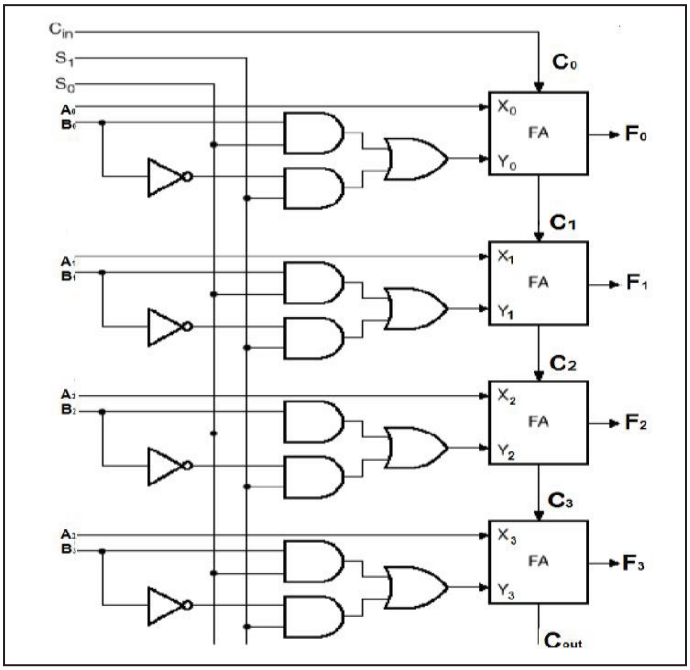


Fig. 4: Logic Diagram of 4 Bit Arithmetic Circuit

The basic block diagram of a logic circuit is shown in fig. 5. For designing logic section multiplexers plays an important role. A 4:1 Mux is used in the logic section. In the logic unit various operations like signed shifts (arithmetic left shift and the arithmetic right shift), logical shifts (logical left shift and the logical right shift), circular shift s (circular left shift and the circular right shift) etc., are performed. With the help of selection lines one of the logic operations is performed.

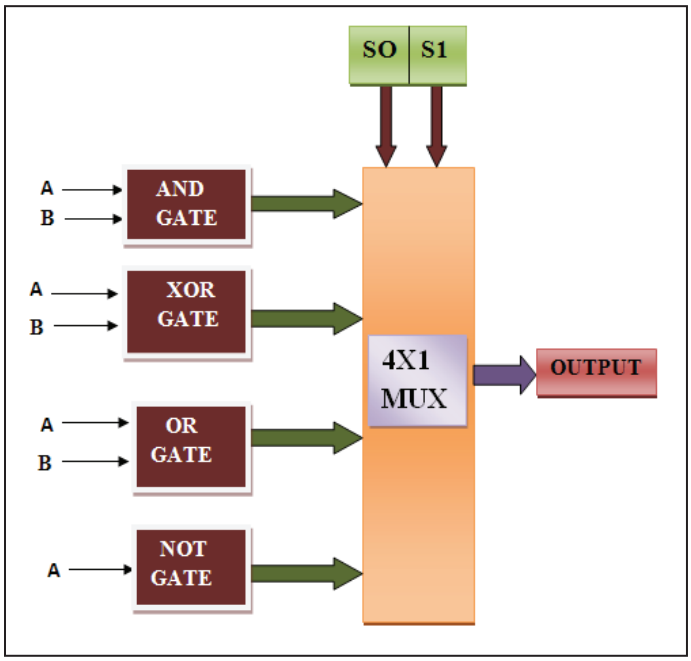


Fig. 5: Block Diagram of a Logic Circuit

The gate level realization of the above discussed arithmetic and logic unit is shown in fig. 6. Using Boolean algebra the outputs are minimised and the total output equations for ALU are

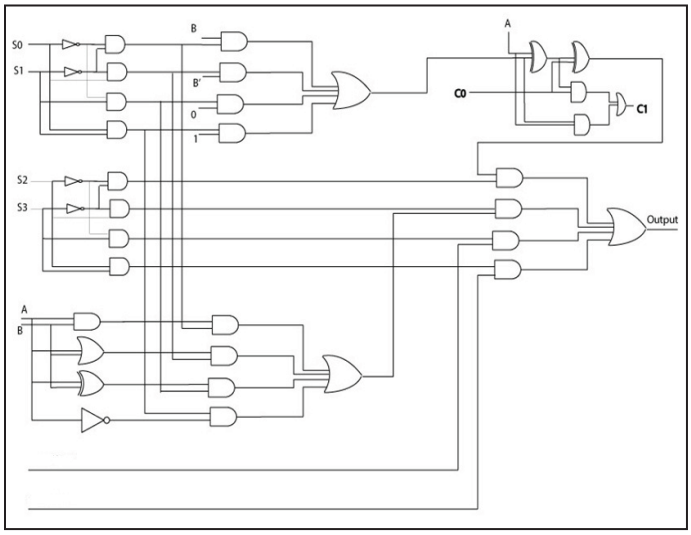


Fig. 6: Gate Level Realisation of 1 Bit ALU CMOS Circuit

T_{out} = (A xnor C_0) B'S_0S_2' + (A xor C_0) B'S_0'S_2' + (A xnor C_0) (B xor S_0) S_1'S_2' + (A xor C_0) (S_0 xor S_1) BS_2' + ABS_1'S_2 + A'$S_0S_1S_2$ + (A xor B) S_0S_1'S_2 + (Axor B) S_0'S_1S_2

C_{out} = S_0'S_1'B(A+C_0)+S_0S_1'A (B'+C_0)+A'C_0S_0(S_1+B')+AS_0'S_1 C_0+AB'C_0S_0'+ S_0S_1

NAND realisation of the resulting circuit is designed completely using nand gates only. Further FAN-IN concept is implemented by increasing the inputs for respective NAND gates. These circuits

are designed in TANNER TOOLS S-EDIT. Power and delay calculations for the respective design is obtained

IV. Results

A. Power Calculations

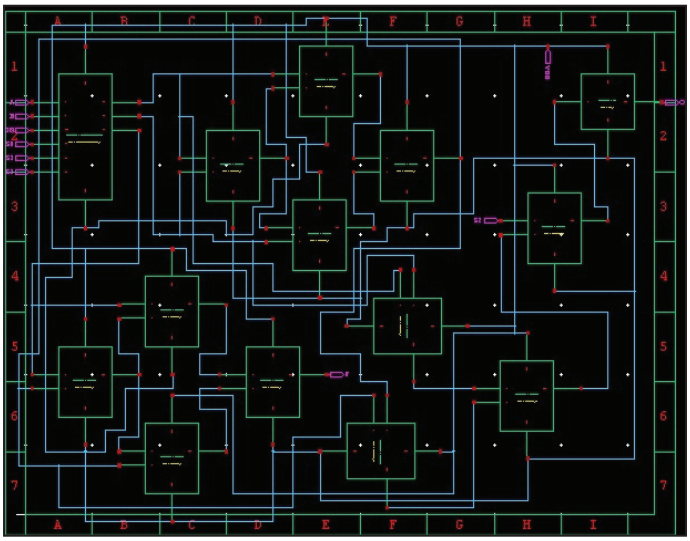
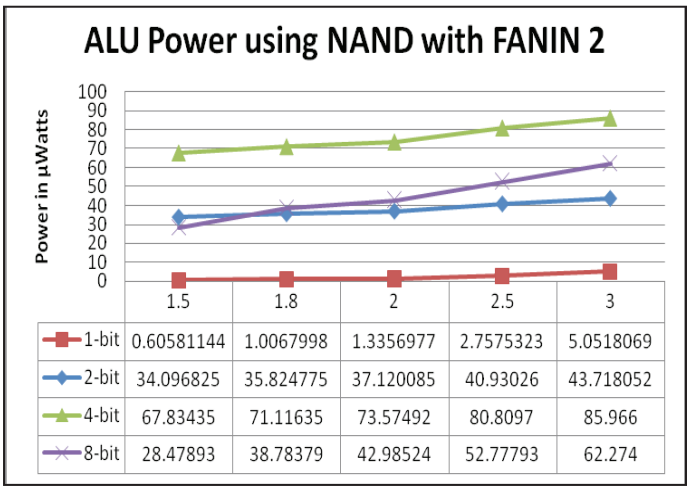


Fig. 7: Simplified Gate Level Realization of 1 bit ALU



	1.5	1.8	2	2.5	3
1-bit	0.60581144	1.0067998	1.3356977	2.7575323	5.0518069
2-bit	34.096825	35.824775	37.120085	40.93026	43.718052
4-bit	67.83435	71.11635	73.57492	80.8097	85.966
8-bit	28.47893	38.78379	42.98524	52.77793	62.274

Fig. 8: ALU Power using NAND with FANIN 2 using NAND gate with FANIN 2

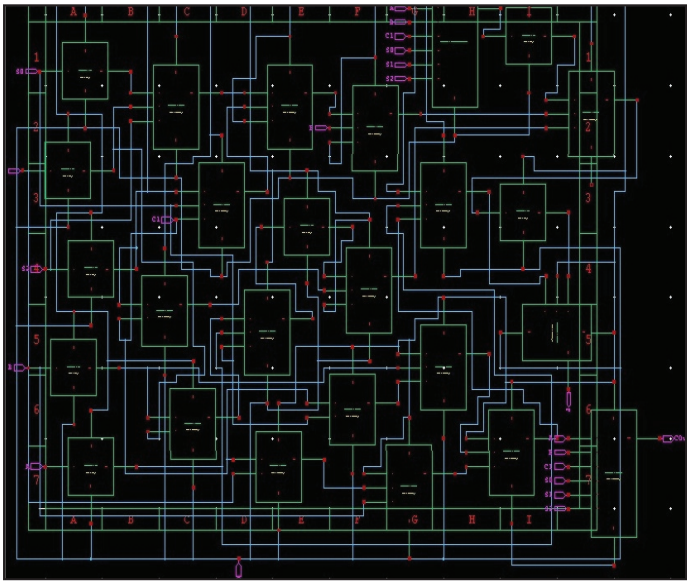
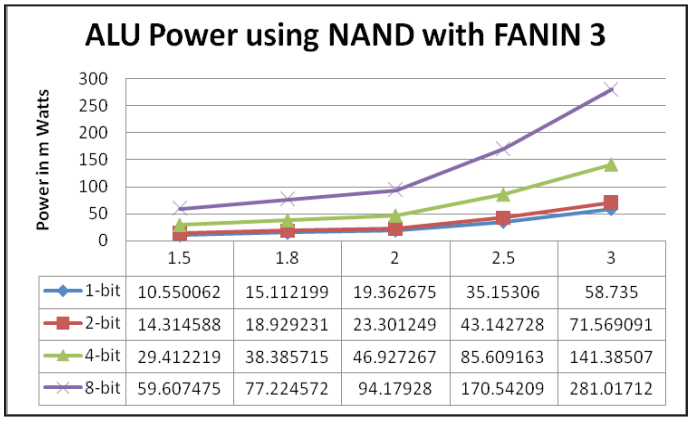


Fig. 9: Simplified Gate Level Realization of 1 bit ALU



	1.5	1.8	2	2.5	3
1-bit	10.550062	15.112199	19.362675	35.15306	58.735
2-bit	14.314588	18.929231	23.301249	43.142728	71.569091
4-bit	29.412219	38.385715	46.927267	85.609163	141.38507
8-bit	59.607475	77.224572	94.17928	170.54209	281.01712

Fig. 10: ALU Power using NAND with FANIN 3 using NAND gate with FANIN 3

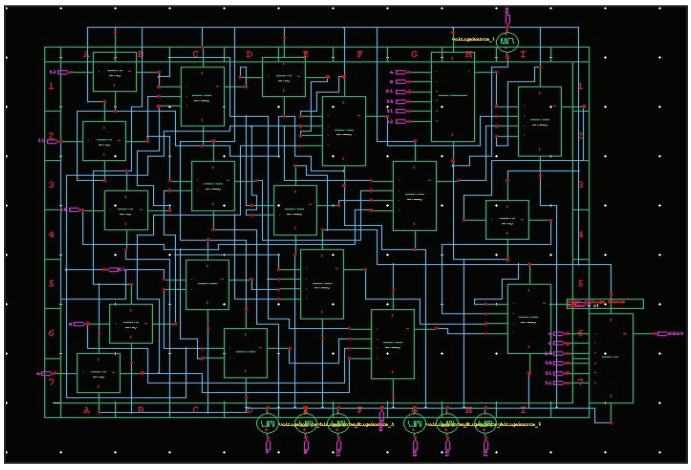
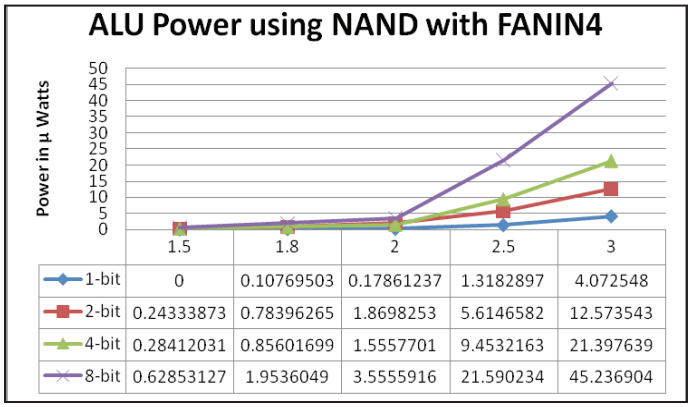


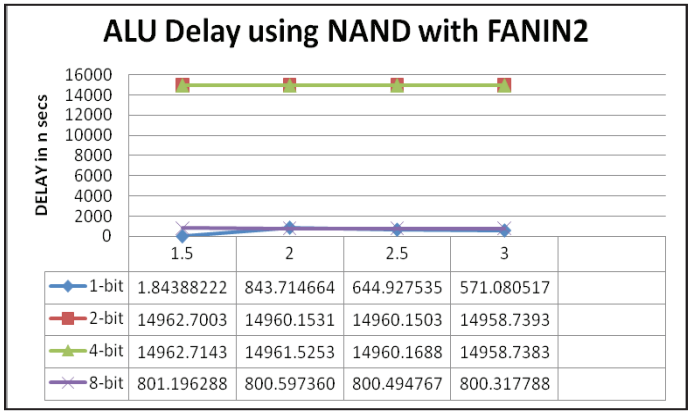
Fig 11: Simplified gate level realization of 1 bit ALU



	1.5	1.8	2	2.5	3
1-bit	0	0.10769503	0.17861237	1.3182897	4.072548
2-bit	0.24333873	0.78396265	1.8698253	5.6146582	12.573543
4-bit	0.28412031	0.85601699	1.5557701	9.4532163	21.397639
8-bit	0.62853127	1.9536049	3.5555916	21.590234	45.236904

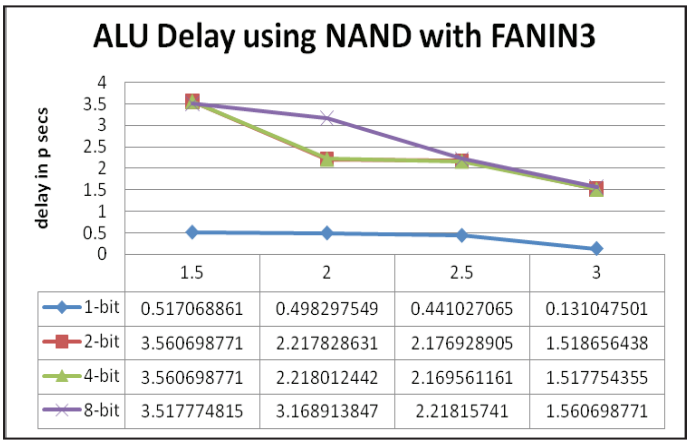
Fig. 12: ALU Power using NAND with FANIN 4 using NAND gate with FANIN 4

B. Delay



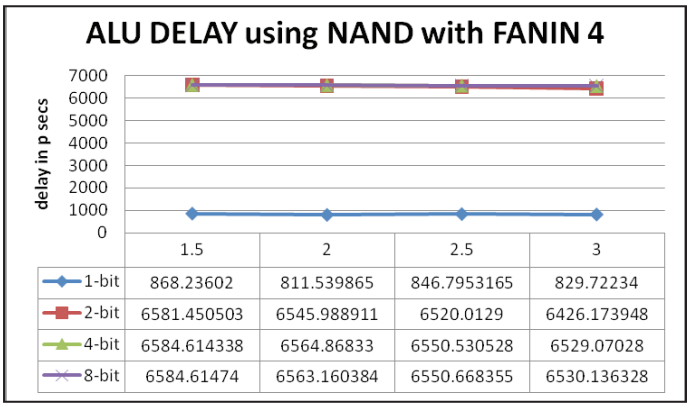
	1.5	2	2.5	3
1-bit	1.84388222	843.714664	644.927535	571.080517
2-bit	14962.7003	14960.1531	14960.1503	14958.7393
4-bit	14962.7143	14961.5253	14960.1688	14958.7383
8-bit	801.196288	800.597360	800.494767	800.317788

Fig. 13: ALU Delay using NAND with FANIN 2



	1.5	2	2.5	3
1-bit	0.517068861	0.498297549	0.441027065	0.131047501
2-bit	3.560698771	2.217828631	2.176928905	1.518656438
4-bit	3.560698771	2.218012442	2.169561161	1.517754355
8-bit	3.517774815	3.168913847	2.21815741	1.560698771

Fig. 14: ALU Delay using NAND with FANIN 3



	1.5	2	2.5	3
1-bit	868.23602	811.539865	846.7953165	829.72234
2-bit	6581.450503	6545.988911	6520.0129	6426.173948
4-bit	6584.614338	6564.86833	6550.530528	6529.07028
8-bit	6584.61474	6563.160384	6550.668355	6530.136328

Fig. 15: ALU Delay using NAND with FANIN 4

V. Conclusion

The circuit designed with NAND realization for 2input, 3input and 4input of 1-bit ALU are presented. Corresponding power calculation values are also presented. Comparing NAND power and delay values, we can observe that by increasing supply voltage the power will increase and delay will decrease. Going into depth we can observe that ALU with FANIN 3 has less delay compared to other designs. The power consumed is less for 1.8VDD when compared to that of 2.5VDD. This is due to the reason that decrease in the VDD results in the reduction of overall power consumed. In this way comparing all the results the low power 1Bit ALU is obtained.

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