Modeling, Simulation and a Relative Study of CNT Bundle with Copper for VLSI Interconnect

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Abstract
The vital innovation scaling in VLSI prompts reduce the extent of chip. Such consistent scaling down of VLSI devices has strong impact on the VLSI advancement in a couple of customs. The interconnect delay turns out to be substantially more colossal and the performance of ICs have been prolonged. Copper interconnects have turned into a huge implementation limiter. Thusly to overcome from the limitation, Carbon Nano tubes have been projected as a conceivable substitution of copper interconnects. This paper displays the extensive investigation on the demonstrating and re-enactment strategies of blended CNT package interconnects. The performance of Mixed CNT interconnects is evaluated and examined against standard Cu interconnects at diverse parameters. The proposed displaying and reproduction methods for CNT interconnect organize are required to assume a vital part later on CNT nanotechnology applications. CNTs indicated 30% change in delay and vitality over copper at the 22 nm nodes and a half increment in all out system throughput for a power obliged on-chip arrange application.

Keywords
CNT, Nanotechnology, SWCNT, VLSI

I. Introduction

The reserved scaling of semiconductor devices in VLSI incorporated infers that there is a substitution of a noteworthy number of the ordinary materials used. Copper interconnect resistivity increases because of surface harshness and particle limit dispersing, resulting increment in propagation delay, control scattering and electro relocation, which is mainly due to scaling the cross section area of the interconnect.

The need to discover elective interconnect arrangements is due to the uprising factor of the restriction experienced in lithography process along with other factors such as electron migration and increasing resistivity. We have seen in the past the materials that offer the capability to carry large current density in nonexistence of electron migration are carbon nano tubes. Basically carbon nano tubes can be classified into two types. If the CNT is the collection of only one thin mass of grapheme sheet then it is known as single walled carbon nano tube (SWCNT). SWCNTs are usually known to have 1-2nm dimension width. On the other hand CNT formed by collection of numerous SWCNTs to represent a grapheme tube are known as multi walled carbon nano tube (MWCNT).

In comparison, it is been observed that due to the low resistivity that SWCNT has to offer, SWCNT have been the decision. SWCNT offers low resistivity because when it is used as an interconnect material it has a longer mean free path.

In accordance to low resistivity, SWCNTs have the potential to uphold high current density without the downside of electro movement issue [2]. Keeping in mind all the benefit SWCNT has to offer, it fits perfectly for the principle of electronic appliances .Furthermore the resistance observed while using SWCNTs for scaling down the device is comparatively low as observed when other metals are used for the purpose of interconnect.

In this paper, I explore the potential effect of CNT over copper as interconnect. The different plan parts of blended CNT package and explores the possibilities of blended heap of CNTs as future interconnects concentrating change on resistivity and system through put.

II. Establishment of CNT Interconnects

There have been many instant to demonstrate the RCL module of SWCNTs. But the demonstrations of various parameters are only frequency dependent.

Let *r* be the radius of the carbon nanotube, let the division between two carbon nanotubes be represented by *d*, and let the length of the carbon nanotube be *l*.

And let the arrangement of carbon nanotube be as shown in the diagram below. Let us also consider the frequency dependent model of SWCNTs represented in terms of R, L and C [1].

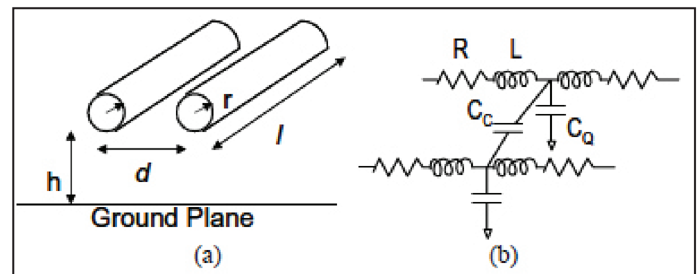

Fig. 1: Frequency Dependent Model of SWCNTs Represented in Terms of R, L and C

Be that as it may, while considering the diffusive segment in the above displayed R, L, C model of SWCNT, resistance was neglected. Under such circumstances the impedance occurring is often known as intrinsic impedance. Intrinsic impedance is also known as contact or quantum resistance. The intrinsic impedance occurring is represented by *h*/*e2*. In the above representation of intrinsic impedance, h denotes Plank's steady and electronic charge is denoted by *e* [7]. However, resistance cannot be neglected when the interconnect length involved are longer along with the high predisposition.

Therefore above consideration are only idealistic presumptions. Electron phonon interconnection becomes a vital part while dealing with interconnect with longer length and higher predisposition. And also we need to keep in mind the impact of scattering.

When multiple, single-walled carbon nanotubes are pressed hexagonally with one another it forms a interconnect of SWCNT package. Individual CNT are surrounded by 6 neighboring CNT as appeared in their center consistently isolated by a separation 'x'. The best execution is accomplished with thickly stuffed structure having 'x'='d' (CNT breadth). The expression gives the aggregate number of CNTs 'nCNT' in the package. The quantity of lines is represented by 'n_h' and 'n_w' denotes the section in the overall bundle.

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$$n_w = \frac{(w-d)}{x};$$

$$n_h = \frac{(h-d)}{\frac{\sqrt{3}}{2}x} + 1;$$

$$n_{CNT} = n_w n_h - \frac{n_h}{2}, \text{ if } n_h \text{ is even} = n_w n_h - \frac{n_h - 1}{2},$$

In the event that nh is odd , 'h' represents the thickness and 'w' represents width of the SWCNT package and for the most part, stature is by and large thrice the width for all advancements.

III. Resistance

The one sided voltage along with the length of the CNT corresponds to the resistance of the bundle. Over the past event, the analysis carried out by Ji-Yong [2], when the interconnect are positioned by a distance of 1.8nm (r=0.9nm) the overall resistance of SWCNT is measured. In this incomprehensible breaking point, we can represent the differential resistance as given by equation below. Considering four channel of conduction and length of the interconnect l which is assumed to be grater than (>λ).

$$\text{For } V < V_{critical}\ R_{diff}^{low} = \frac{dV}{dI} = \left(\frac{h}{4e^2}\right)\Theta\left(\frac{l}{\lambda_{low}}\right)$$

$$\text{For } V > V_{critical},\ R_{diff}^{high} = \frac{dV}{dI} = \left(\frac{h}{4e^2}\right)\Theta\left(\frac{l}{\lambda_{high}}\right)$$

where,

$$\Theta(x) = 1 \text{ for } x<1$$
$$= x \text{ otherwise}$$

$$\lambda_{low} = \lambda_{acc} \text{ and } \lambda_{high} = (\lambda_{op}^{-1} + \lambda_{zo}^{-1})^{-1}.$$

Where,
V is the applied voltage,
I represent the current flowing through the CNT,
λ is the mean free way (mfp)

When l < λ, (h/4e2) derives for quantum resistance given for all four channels [10]. Only the deferential resistance of SWCNT is depicted by the above mentioned equation. However it is equally important to establish the net resistance of the system also known as the dc resistance. Net resistance is given as below:

For V< $V_{critical:}$

$$R^{low} = R_{diff}^{low}$$

For V> $V_{critical}$

$$R^{high} = \left(\frac{V_{critical}}{V_{bias}}\left(\frac{1}{R_{diff}^{low}} - \frac{1}{R_{diff}^{high}}\right) + \frac{1}{R_{diff}^{high}}\right)^{-1}$$

Accordingly, in order to calculate the net resistance we have built up a resistance model. This resistance model is obtained keeping in mind length and bias dependent resistance and also examining the experimental parameters. Quantum resistance constraint is brought about while dealing with shorter length of the nanotubes. The quantum resistance constrains are also known as ballistic transport. At an estimation of about 25 µA the current saturates while considering the longer length of carbon nanotubes [2]. SPICE simulation software is utilized for recreation of resistance model of the circuit. The contact limitation additionally prompts a substantial estimation of resistance. SWCNT resistance of 6-100 kΩ has been accounted for. The frequency-independent resistance model show has been checked and the results are showed up in fig.

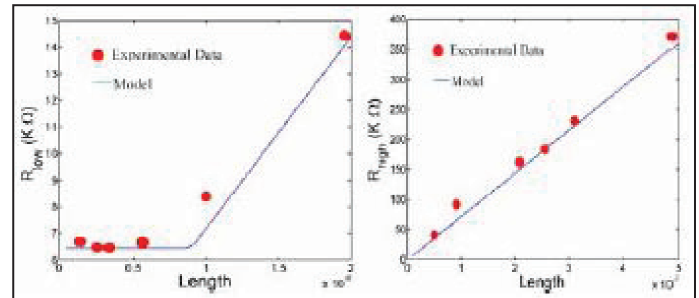

Fig. 1: Differential Resistance of a CNT (a) for Low Bias (b) for High Bias

IV. Capacitance

The net effective capacitance is the series arrangement of quantum capacitance of the overall bundle. The electrostatic energy that is stored in the carbon nano tube is represented by the quantum capacitance, while conveying the current along with the electrostatic capacitance of SWCNT package due to charge stored by SWCNT. There are two distinct capacitance that are to be considered [12].

Namely, Electrostatic Capacitance (CQ) and Quantum Capacitance (CC) [3]. When the capacitance is taken between the ground plane and a wire and when capacitance occurs due to the charger stored by the ground plane of the CNT it is called as Electrostatic Capacitance (CQ). The energy stored in terms of the capacitance are given below:

$$C_Q = \frac{2\pi\varepsilon}{\cosh^{-1}(2h/d)} \approx \frac{2\pi\varepsilon}{\ln(h/d)}$$

$$C_C = \frac{2e^2}{hv_F}$$

Where,
ε is the permittivity,
h is the height of the nanotubes from ground plane
d is the separation between two parallel nanotubes

The above condition is legitimate for h>2d.

V. Inductance

Each single CNT corresponds to its inductance. The parallel combination of all single CNT inductance corresponds to the inductance of SWCNT bundle. Similar to capacitance of SWCNT bundle, there exist two inductance of SWCNT bundle [3]. Namely, magnetic inductance and kinetic inductance. Initially, the magnetic inductance per unit length between CNT and ground plane is given as,

$$L_M = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{2h}{d}\right) \approx \frac{\mu}{2\pi}\ln\left(\frac{h}{d}\right)$$

The above condition is legitimate for h>2d. Usually, a protective layer (regularly, silicon dioxide) is present on top of CNT. The usual diameter of the substrate is between 10mm and 1, where as for nanotubes the radius ranges from 1nm-2nm. The magnetic

inductions are the direct effect of the capacity factor (h/d). The magnetic inductance is discovered to be around 1nH/μm under normal geometrical parameters.

While considering single dimension inductance, kinetic induction play equally vital role as magnetic induction. The kinetic inductance is derived similar to magnetic inductance and is gives as [6],

$$L_K = \frac{h}{2e^2 v_F}$$

Where v_F, denoted the fermi speed. Typically 8×10^5 m/scan be taken as the Fermi speed for CNT. Kinetic Inductance is constantly prevailing and essential in circuit investigation. The typical estimations of these two capacitances are comparative [11].

In this way, both these two sorts of capacitance are critical amid investigation.

$$\frac{L_M}{L_K} = \alpha \frac{2}{\pi} \frac{v_F}{c} \ln(\frac{h}{d}) \approx 10^{-4}$$

Where α is the fine structure constant which is approximately equal to 1/137.

VI. Correlation of Cu and CNT Interconnect

Due to shorter free mean path of the electron, it is observed that resistance and inductance for SWCNT is comparatively higher than that for copper [5]. If there should be an occurrence of copper accordingly they experience progressive collisions at scaled innovation lengths. It is observed that the power dissemination is higher under such situation due to higher capacitance of SWCNT then that of copper.

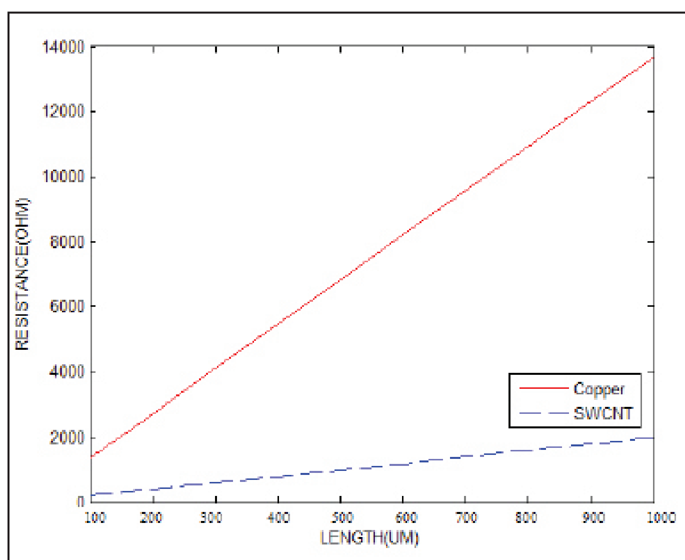

Fig. 1: Comparison of Resistance between SWCNT and Copper

From the above graph, it is clearly evident that the resistance of CNT is smaller than that of copper. The higher resistance is due to the fact that electrons are more scattered in Cu surface. There is a sharp rise in the resistivity due to the high resistive diffusion barrier layer.

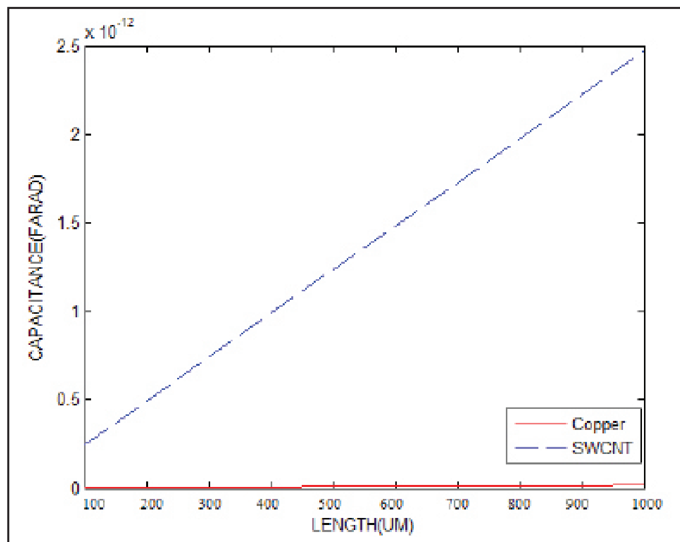

Fig. 2: Comparison of Capacitance between SWCNT and Copper

As SWCNT has less estimation of resistance and capacitance in contrast with copper, SWCNT has less propagation delay. The estimation of resistance and capacitance increments with length, thus delay is likewise increment with interconnect length for copper and half breed interconnect [9].

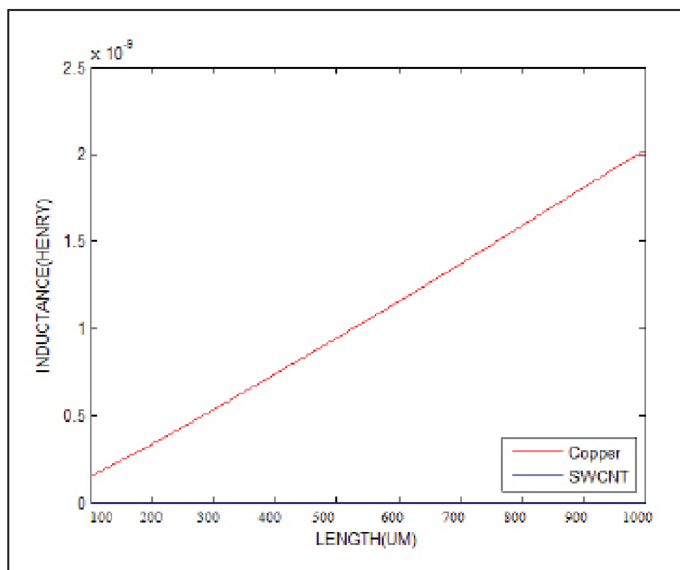

Fig. 3: Comparison of Inductance Between SWCNT and Copper

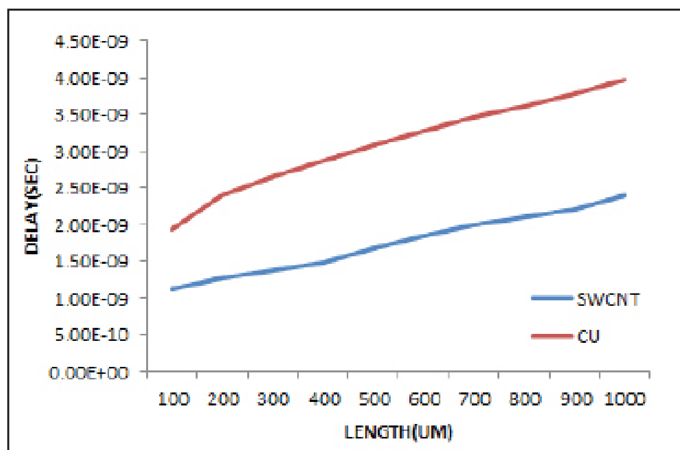

Fig. 4: Delay Analysis between SWCNT and Copper

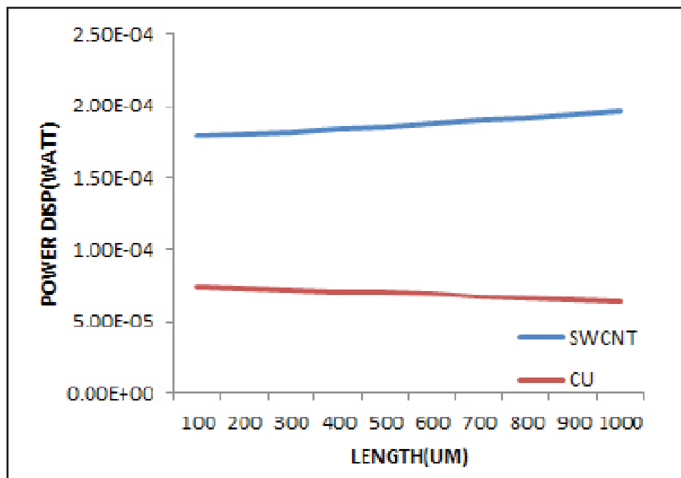

Fig. 5: Power Analysis between SWCNT and Copper

Due to higher value of capacitance, SWCNTs experiences more power dissipation. However the capacitance of SWCNT can be reduced by altering other parameters such as width [6].

When the width of the nanotubes is increased, capacitance can be reduced. Thus, examining all the parameter factors it is advisable to conclude that SWCNT can serve as a superior material in VLSI interconnect application when the vital innovation scaling in VLSI is taking place.

VII. Conclusion

It has been observed that if the width and the thickness of the CNT bundle is altered then the resistance of the CNT bundle can be rationalized. Additionally it is also observed that delay and energy delay product of CNT beats the Cu interconnect performance. Thus we can conclude that CNT has a wide range of potential and can substitute copper given the circumstances of constraint of copper. To sum things up, the examinations and reenactments detailed by different creators demonstrate that if a CNT innovation good with show type of IC innovation can be produced, at that point it will be conceivable to in part or completely supplant copper interconnect by CNT based interconnect.

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