Design and Implementation of High Speed Multiplier Using Adiabatic Logic

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Abstract
In VLSI Design Area Power consumption is an important issue. In high performance systems Multipliers are having a major role. One of such multiplier is The Wallace tree multiplier. It is faster than a simple array multiplier and is an efficient implementation of a digital circuit. This multiplier which is effective both in terms of speed and power. One of an attractive solution for low power electronic applications is Adiabatic logic style. By using this technique energy dissipation in PMOS network can be minimized and some amount of energy stored at load capacitance can be recycled instead of dissipated. In this paper ECRL(Efficient Charge Recovery Logic) based Wallace tree multiplier is compared with conventional logic based Wallace tree multiplier. Tanner EDA tools are used for simulation.

Keywords
Wallace Tree Multiplier, Adiabatic Logic, Efficient Charge Recovery Logic

I. Introduction

In Today's Digital Signal Processing And Various Other Applications Multipliers play an important role .For example microprocessor, dsp etc. addition and multiplication are most often used arithmetic operations. Statics shows that more than 70% instructions in microprocessor and dsp algorithms perform addition and multiplication. mostly these functions dominates the execution time. so there is a need of high speed multiplier and the demand of high speed processing has been increasing as a result of expanding computer and signal processing applications.

Another important issue in multiplier design is power consumption. To achieve low power consumption it is good to reduce the number of operations. Therefore the dynamic power which is a major part of total power consumption is reduced. So the need of high speed and low power multiplier has increased. The objective of a good multiplier is to provide a physically packed together, high speed and low power consumption unit. First part of this paper different types of multipliers are described: Booth multiplier, sequential multiplier, combinational multiplier, wallace tree multiplier. In next section different techniques used in mac for efficient operations are discussed.

A. Wallace Tree Multiplier-An introduction

A Wallace tree multiplier is an efficient hardware implementation of a digital circuit that multiplies two integers devised by an Australian computer scientist Chris Wallace in 1964. Wallace tree reduces the no. of partial products and use carry select adder for the addition of partial products.

Three steps in Wallace tree:-

- Multiply each bit of multiplier with same bit position of multiplicand. Depending on the position of the multiplier bits generated partial products have different weights.
- Reduce the number of partial products as two by using layers of full adders and half adders.

After second step we get two rows of sum and carry, add these rows with conventional adders.

- As long as there are three or more rows with the same weight add a following layer:

Make any three rows with the same weights and input them into a full adder. The result will be an output row of the same weight i.e. sum and an output row with a higher weight for each three input wires i.e. carry.

If there are two rows of the same weight left, input them into a half adder.

If there is just one row left, connect it to the next layer. The advantage of the Wallace tree is that there are only O (log n) reduction layers (levels), and each layer has O (1) propagation delay. As making the partial products is O (1) and the final addition is O (log n), the multiplication is only O (log n), not much slower than addition (however, much more expensive in the gate count). For adding partial products with regular adders would require O (log n2) time.

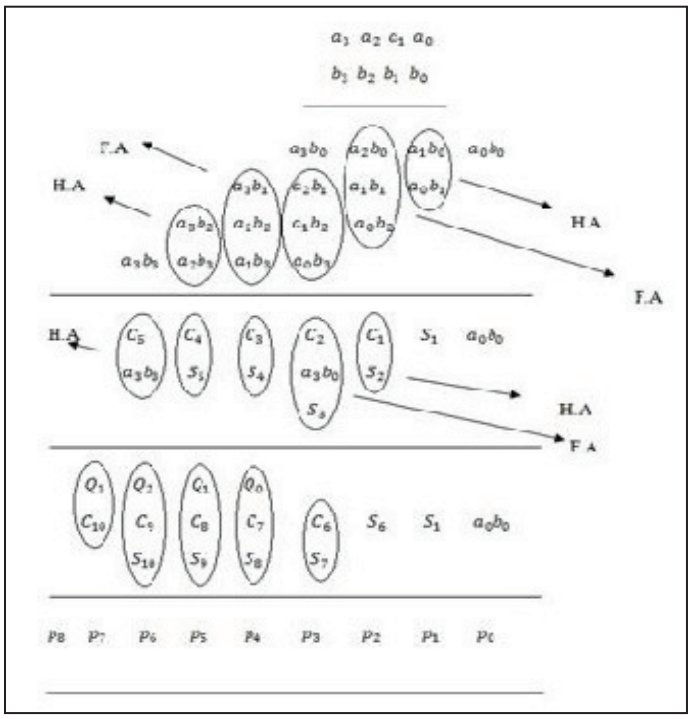

Fig. 1: 4x4 Wallace Tree Multiplier

This reduction method is applied to each successive stage until only two rows remain. This process is illustrated by the conventional 4- bit by 4-bit Wallace multiplier as shown in fig.1.The reduction is performed in four stages. The third phase will require a (2N-1-S) wide adder, where s-number of stages in reduction.

B. Conventional Multiplier

A 4bit * 4bits booth-encoded Wallace tree multiplier are implemented in verilog to demonstrate the proposed multiplier.

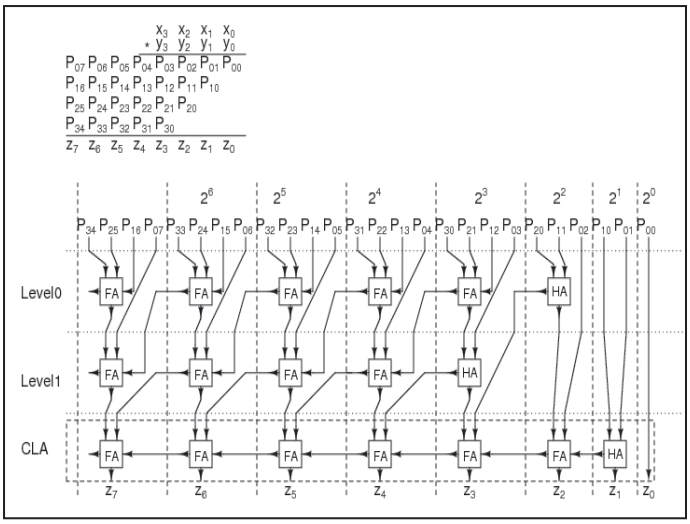

Fig. 2: Conventional Multiplier

According to the figure above, the wallace tree only need 18 adders (15 Full-adders and 3 Half-adders). The typical array multiplier might need 64 Adders for signed multiplication. This can have substantially area-saving.

II. About Adiabatic Logic

Adiabatic Logic is the term given to low-power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. The term adiabatic logic is used in low-power VLSI circuits which implements reversible logic. In this, the main design changes are focused in power clock which plays the vital role in the principle of operation.

A. CMOS Adiabatic Circuits

Adiabatic circuits are low power circuits which use "Reversible Logic" to conserve energy.

Traditional CMOS circuits dissipate energy during switching, But adiabatic circuits reduce dissipation by following two key rules:

- Never turn on a transistor when there is a voltage potential between the source and drain.
- Never turn off a transistor when current is flowing through it.

While this is an area of active research, current techniques rely heavily on transmission gates and trapezoidal clocks to achieve these goals.

The classical approaches to reduce the dynamic power are reducing supply voltage, decreasing physical capacitance and reducing switching activity. These are not fit enough to meet today's power requirement. However, most research has focused on building adiabatic logic, which is a promising design for low power applications.

Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply.

B. 2N2N-2P Function Block

The design of high-speed and low-power VLSI architectures needs efficient processing units, which are optimized for the speed and power consumption. Hence, the techniques to reduce the power dissipation, low power operation, and designing for energy recovery and recycling are most needed. Energy recovery is proving to be a promising approach for the design of low power VLSI circuits. The primary advantage of these circuits results from its inherent characteristics of deriving a constant current from the power clock get the FETs working with the minimum voltage between the source and drain terminals. The basic complementary function Block of 2N-2N2P.

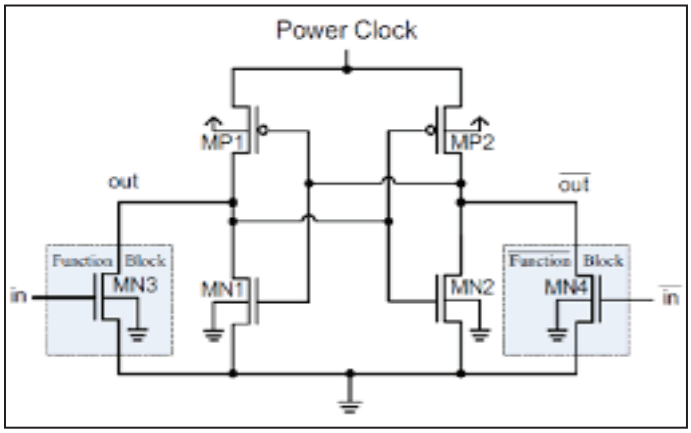

Fig. 3: Function Blocks 2N2N-2P

1. 2N2N-2P Logic

The name 2N-2N2P is based on the convention of using the number of transistors in the inverter gate. Figure 1 illustrates the CMOS circuit of 2N-2N2P XNOR/XOR logic. Since there are energy losses due to nonzero voltage drop needed to turn on unidirectional devices, 2N-2N2P is covered under partial Energy Recovery Logic (ERL) family. 2N-2N2P has cross-coupled inverters to latch the output. 2N-2N2P is a revised version of Efficient Charge Recovery Logic (ECRL). Similar to ECRL, the pull-down network, which is helpful in fast discharging during the evaluation phase, is complementary to each other.

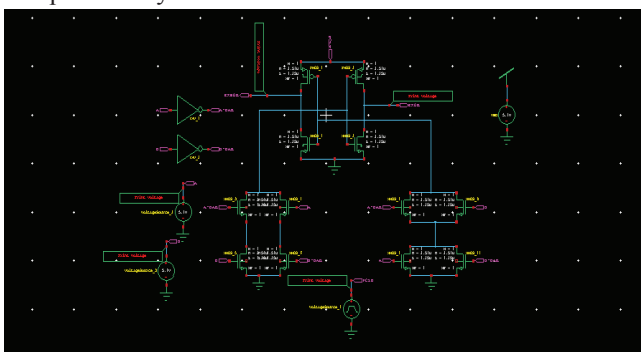

Fig. 4: Ex-or Gate 2N2N-2P

B. 2N2N-2P WALLACE TREE MULTIPLIER

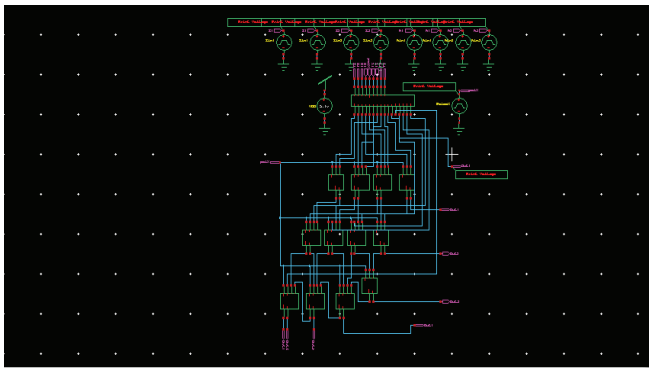

Fig. 5: 2N2N-2P Wallace Tree Multiplier

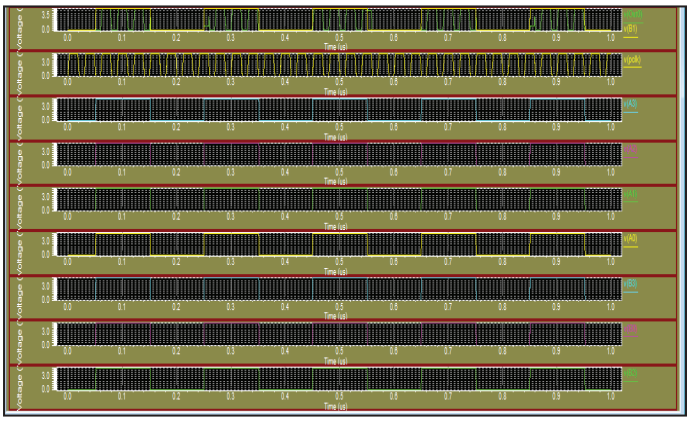

Fig. 6: 2N2N-2P Wallace Tree Multiplier Output Waveform

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* BEGIN NON-GRAPHICAL DATA

Power Results
VVDD from time 0 to 1e-006
Average power consumed -> 1.053192e-001 watts
Max power 4.231218e-001 at time 1.51653e-007
Min power 5.411383e-007 at time 0


* END NON-GRAPHICAL DATA
*
* Parsing                    0.01 seconds
* Setup                      0.09 seconds
* DC operating point         0.59 seconds
* Transient Analysis        19.31 seconds
* Overhead                   1.41 seconds
* ---------------------------------------
* Total                     21.41 seconds

* Simulation completed

* End of T-Spice output file
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Fig. 7: 2N2N-2P Wallace Tree Multiplier Power Result

In this 2N2N-2P Wallace tree multiplier can improve speed and power consumption. It will be implemented in several application like computer, cell phone etc.

III. Comparison Table

Table 1: Comparison of Adiabatic Logic and Conventional Logic Based Wallace Multiplier

Name of the Design	Conventional logic(Watts)	Adiabatic logic (Watts)
And Gate	9.90712*10-5	0.11971*10-5
Or Gate	6.46538*10-6	1.52658*10-6
XOR Gate	1.85029*10-4	0.01656*10-4
Half Adder	4.03740*10-4	3.58102*10-4
Full Adder	5.17932*10-4	0.01525*10-4
Wallace tree	6.08188*10-3	1.0531*10-3

IV. Conclusions

It is concluded from above comparison that energy consumption at lower frequencies is minimum in case of ECRL followed by CMOS, 2N2N2P i.e. leakage losses are minimum in ECRL. As the frequency of operation increases energy consumption starts decreasing At above process remains no longer adiabatic as a result energy consumption of all three adiabatic techniques becomes greater than CMOS. Frequency of operation of adiabatic logic could be increased to few hundred of MHz if load capacitance is reduced. Area consumption of adiabatic logic is greater than standard CMOS which its main disadvantage. Thus the applications are limited, for example a pace maker where energy saving is main target.

In future, 2N2N-2P ECRL LOGIC will be implemented in DADDA TREE MULTIPLIER to improve speed,power consumption etc.

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