# Design of 4 Bit FLASH Analog to Digital Converter Using TM Comparator Circuit and Gray to Base2 Encoder using 0.13µm CMOS Technology

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**Abstract**
As communication mainly done in the form of digital data, the applications for ADCs increases Analog-to-Digital converters are needed in all those applications, which interface with the analogue world and exploit the digital processing of data. As digital processing is more and more gaining ground over analogue signal processing, the importance of Analog - to- digital converters correspondingly increases. The Flash type ADC, also known as Direct Conversion ADC, uses a bank of comparators, operating in parallel to achieve a high data conversion rate. In this paper, an area efficient low power high Speed 4-bit Flash Type ADC using gray to base-2 encoder is proposed in 130 nm CMOS technology. The concept of Threshold Modified Comparator Circuit (TMCC) is also introduced as a modification of the conventional comparator. The proposed design of the ADC occupies an active area of 0.0036 mm2 and consumes 43.146 pW of average power while operating with an input frequency of 10 MHz and a supply voltage of 1.8 Volt.

**Keywords**
Flash Type ADC, Comparator, TMCC, Threshold Voltage, Multiplexer, Bit Referenced Encoder, Gray to Base2 Encoder

## I. Introduction

Analog circuits may face the more power constrained situations. Designing of Microprocessor and SoC suffer from power dissipation. The Power Dissipation (PD) is inverse proportional to the square of scaling factor (k).

PD(Digital) ∞1\ k 2 (1)

However,by keeping constant band width,the analog power of CMOS flash ADC scales with the inverse of scaling factor [3].

Analog Power ∞ k-1 (2)

As the technology goes on increasing The digital power scales faster than the analog power, its leads to improve the performance of simple, low resolution analog circuits in ADCson great deal of research on digital techniques .It resulting in mixed signal circuits [3].

The flash type ADC architecture is mostly used because it consist of bank of comparators which are operated in parallel in its architecture. That's why this type of ADCs are more suitable for high speed operations, but this architecture is not power efficient. Flash type ADC is the most appropriate ADC,when we talk about latency.The offset voltage is most parameter in comparators. As the Flash ADCs uses bank of comparators, there may be a chance of random mismatches between the comparators, it leads to random offset of comparators.The output of the ADCs is distorted by non-linearity of ADCs transfer function because of this random offset. As the resolution increases the number of comparators used in Flash ADCs increases, consequently area will be increases due to large number of transistors.The power dissipation is a critical parameter, while designing the analog circuits we must take care about of this parameter. The resistor network used in conventional Flash ADCs consumes more static power.

The performance of an ADCs depends upon high speed, low power and low area etc. resistor bank of the Flash ADC can be replaced with different techniques, in them TIQ technique is used to reduce the static power dissipation[13]. For low power design, a capacitive interpolation technique is used [4]. The power consumption is also reduced by reducing the amplifier used on application of an average termination circuit [5].

The resistor network in conventional Flash ADC is replaced by TIQ comparator but it suffers from the input frequency. To overcome this frequency restriction, a CMOS inverter comparator is proposed in [malathi9]. Even though the requirement of external circuitry increases, consequently the area and power will increases.

A modified inverter based comparator is proposed for Flash ADCs [1] to reduce the power consumption. But an external voltage generator is used for reference voltage, it will leads to more area. So this not suitable for area constrained applications. A Flash ADCs using bit reference encoder [2] proposed for high speed applications. Bit reference encoder is implemented using Multiplexers, whose selection lines are provided by the comparators. There may be a chance of distorted output if any mismatch occurs, as the number of bits increases the size of mux increases. So for low power and area constrain applications it is not suitable. In this paper a 4 bit flash ADC is designed for high speed and low power applications.

## II. Different types of comparators

### A. Inverter Based Comparator

As the name suggest this comparator is designed using inverters along with transmission gates which are used as a switches and a capacitor plays a role of sampler shown in the below fig. 1. The inputs of these comparators are vin and vref and pi. The pi is used as a clock driver which turns on and off the transmission gates. In this arrangement two clock are used which are trigger by pi input named as clk and clkbar called as sample and conversion clocks respectively. The switching threshold voltages for all inverters are vdd/2. It operated in two phases.

Sampling phase (when clk is asserted i.e., pi = 1), during this phase the transmission gates which is having clk = 1 are opened remaining transmission gates are closed. At this time of instant the input vin is sampled by using capacitor. The equation of voltage across the capacitor

$$V_c = V1 - Vx \quad (1)$$

$$Vc = V_{dd} - Vin \quad (2)$$

Since the transmission gate 4 is open, the latch structure will be formed by the inverter i2 & i3. This latch stores the previous sampled output. Hold phase(when clkbar is asserted i.e., pi = 0) in this phase all transmission gates except 2 & 4 are open. In this condition the reference voltage is connected to input plate of the capacitor. Now the voltage across capacitor becomes

$$V_c = V1 - Vref \quad (3)$$

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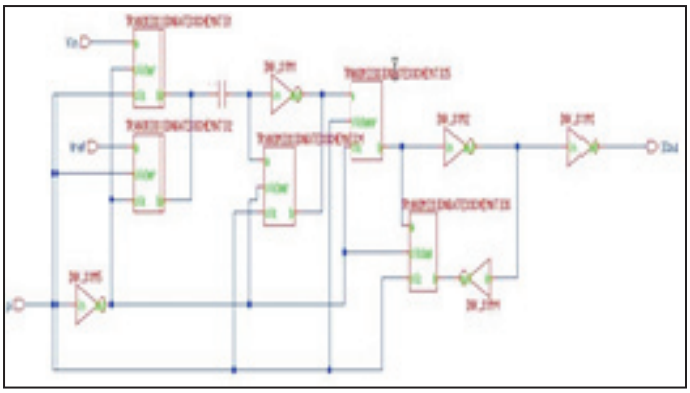

Fig. 1: Inverter Based Comparator

Vi = Vc + Vref = (Vdd/2 -Vin) + Vref
= Vdd/2 - (Vin - Vref)

Now the comparator compare the previously stored input data with instantaneous reference voltage gives the difference. The autozeroing is not used in this arrangement.

### B. TMCC

TMCC stands for Threshold Modified Comparator Circuit, as name implies it uses the threshold voltage as reference voltage. Threshold voltage will be varied for all the transistors which are having different width and length ratio and vice versa. TMCC is consisting two inverters. The input is connected to the inverter whose threshold voltage is modified and the output is connected to a NOT gate is shown in below fig. 2.

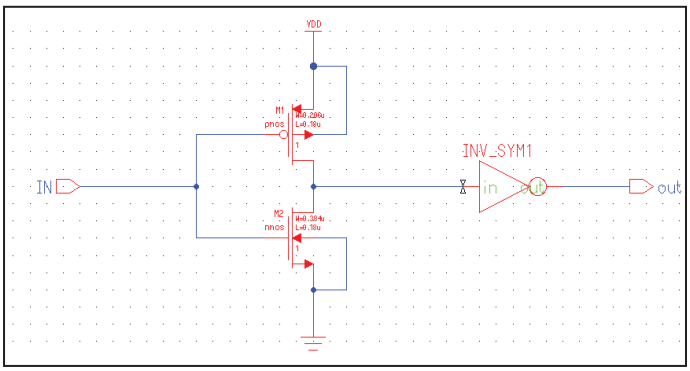


Fig. 2: Threshold Modified Comparator Circuit

Depending upon reference voltage the width and length ratios of NMOS and PMOS transistors will be changed. The threshold voltages of all TMCCs are calculated by using above equations by changing the W\L ratio of NMOS and PMOS respectively. The modified threshold voltages for each and every NMOS and PMOS transistors along with width and lengths are listed in below table

Table 1: Vth along with width and length of PMOS and NMOS transistor

| TMCC | Threshold voltage (volts) | Wn (µm) | Ln (µm) | Wp (µm) | Lp (µm) |
|---|---|---|---|---|---|
| 1 | 0.500 | 0.384 | 0.13 | 0.206 | 0.13 |
| 2 | 0.538 | 0.325 | 0.13 | 0.200 | 0.13 |
| 3 | 0.576 | 0.282 | 0.13 | 0.200 | 0.13 |
| 4 | 0.614 | 0.218 | 0.13 | 0.200 | 0.13 |
| 5 | 0.652 | 0.246 | 0.13 | 0.200 | 0.13 |
| 6 | 0.690 | 0.192 | 0.13 | 0.200 | 0.13 |
| 7 | 0.728 | 0.171 | 0.13 | 0.200 | 0.13 |
| 8 | 0.766 | 0.240 | 0.13 | 0.318 | 0.13 |
| 9 | 0.805 | 0.210 | 0.13 | 0.312 | 0.13 |
| 10 | 0843 | 0.210 | 0.13 | 0.350 | 0.13 |
| 11 | 0.881 | 0.210 | 0.13 | 0.390 | 0.13 |
| 12 | 0.919 | 0.200 | 0.13 | 0.420 | 0.13 |
| 13 | 0.957 | 0.200 | 0.13 | 0.472 | 0.13 |
| 14 | 0.995 | 0.190 | 0.13 | 0.501 | 0.13 |
| 15 | 1.002 | 0.180 | 0.13 | 0.537 | 0.13 |

Actually the inverter at input side is do the comparison gives the reverse output i.e., when vin is greater than vref then output is logical 0, For vin is less than vref output is logic 1.That's why another inverter is kept at output side for correct output.

## III. Different Types of Encoders

### A. Gray to Binary Encoder

In conventional flash type ADCs the input is not directly converted to binary code, some intermediate stepsare employed. Those are first converted to thermometric code, these are corrected and then converted to gray code and finally to binary. But now we eliminate those intermediate steps and do the direct conversion to the gray and then to binary in order to remove the redundancy of first generating the thermometric code and then the gray code.

The gray to binary code converter circuit is shown in below fig. 3. It consists three EX-OR Logic gates taking gray code bits G3,G2,G1,G0 as inputs and D4,…D1 binary outputs.

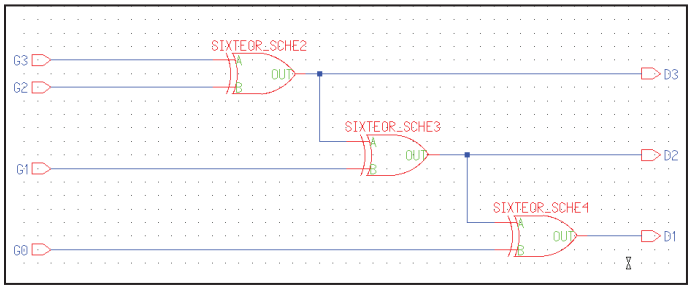


Fig. 3: Schematic Diagram of Gray to Binary Converter

### B. Bit Reference Encoder

This is another type of encoder which converts the outputs of comparator to binary codes. It is constructed by using multiplexers from truth table. Depending upon number of bits the combination of MUXs will be varied. The thermometric code bits from the comparators used as selection bits and data bits for multiplexers.

Let us consider 3Bit flash ADC, then the comparator outputs are taken as C1, C2…..and D1, D2, D3are the final ADC outputs. Now the relation between the comparator outputs and ADC outputs,we can write the following relations

For
Output = 000, input C4 = 0, C6= 0 & C7= 0.
Output = 001,input C4 = 0, C6= 0 & C7= 1.
Output = 010, input C4 = 0, C6= 1 & C5 = 0.
Output = 011,input C4 = 0, C6= 1 & C5 = 1.
For
Output = 100,input C4 = 1, C2= 0 & C3= 0.
Output = 101, input C4 = 1, C2 = 0 & C3 = 1.
Output = 110, input C4 = 1, C2 = 1 & C1 = 0
Output = 111,input C4 = 1, C2 = 1 & C1 = 1

On observing the above relational expressions one can say that the bit reference encoder is constructed by using one 2 by1 mux and one 4 by 1 mux is shown in below figure.

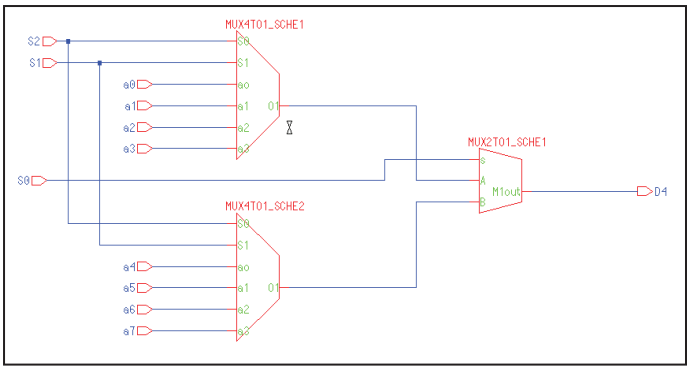


Fig. 4: Schematic for 3 bit Reference Encoder Circuit

## IV. Flash ADCs

### A. Flash ADC Using Inverter Based Comparator

In this architecture the conventional comparators are replaced by modified inverter comparator. Operations of all ADCs are equal, but the sampling and conversion process are different, in this type of the operation of ADC is performed in two phases.

In first phase the analog input is sampled and stored in capacitor when the clock is at high logic level known as sampling phase. During the second phase the clock input goes to low logic level, then the second input i.e. reference voltage is compared with previously stored input samples and corresponding thermometric code will be generated at the outputs of comparators. These codes are directly converted to gray codes and final to binary codes. The schematic diagram for this ADC is shown in below fig. 5.

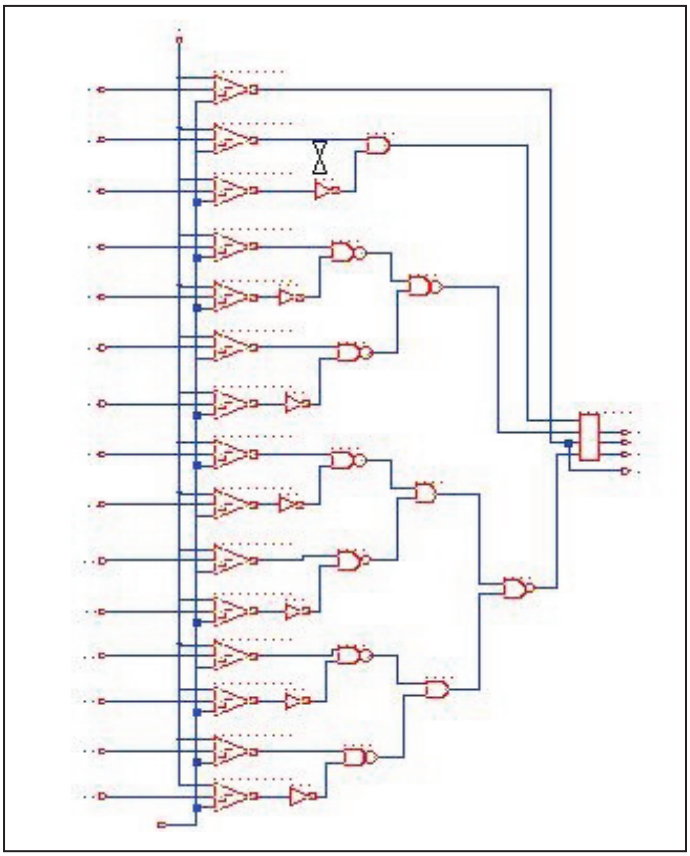

Fig. 5: Schematic Diagram of Modified Inverter Based Flash ADC

The simulated waveform for inverter based flash ADC is shown in below fig. 5. This ADC is simulated in 130nm technology in mentor graphics tool. The ramp type signal is taken as input for this ADC, the output look likes below

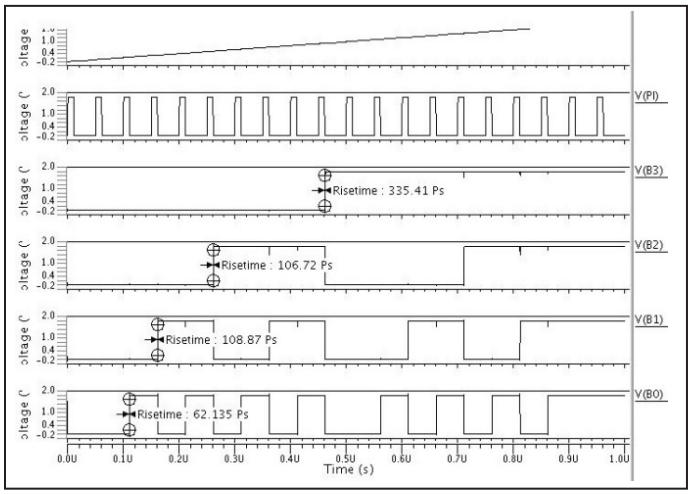


Fig. 6: Simulation Results for Modified Inverter Based Flash ADC

### B. Using TMCC and Bit Reference ENCODER

This type of flash ADC structure consists of 7 TMCCs and one bit reference encoder as shown in below fig. 7.

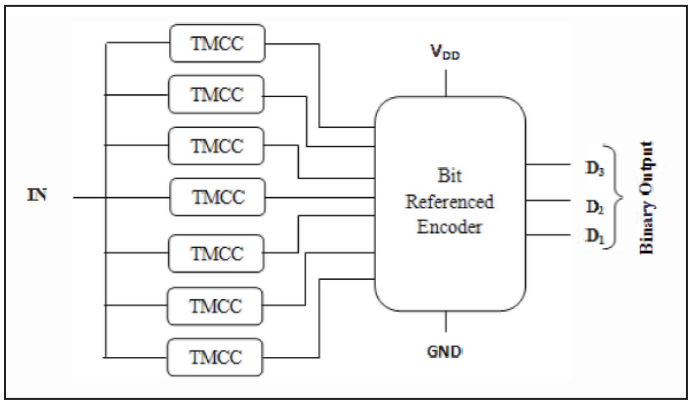


Fig. 7: Block Diagram of Flash ADC with TMCC and Bit Reference Encoder

This ADC is uses the 1.8v Vdd, thus this voltage is divided into 8 levels each level is of 0.225 volts. The incoming analog voltage is compared with all 7 TMCCs reference voltages and finally gives the binary output at the bit reference encoder output side. This Flash ADC is extended to 4 bit flash type ADC. The analysis is as follows: For 4bit ADC we need 15 TMCCs, consequently the outputs also increases .The relationship between outputs of comparator and ADC is listed as in below Table 2.

Table 2: Outputs of Comparators and Flash ADC

| Outputs of comparators | | | | | | | | | | | | | | | Outputs of ADC | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| O1 | O2 | O3 | O4 | O5 | O6 | O7 | O8 | O9 | O10 | O11 | O12 | O13 | O14 | O15 | D1 | D2 | D3 | D4 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |

By analysing the above table we can deduce the selection and data lines for MUXs, which are used to implement the 4bit Bit Reference Encoder.

For

Output = 0000: O8 = 0, O12= 0, O14=0& O15= 0.
Output = 0100: O8 = 0, O12= 1, O14=0 & O11= 0.
Output = 0001: O8 = 0, O12= 0, O14=0 & O15= 1.
Output = 0101: O8 = 0, O12= 1, O14=0 & O11= 1.
Output = 0010:O8 = 0, O12= 0, O14=0 & O13= 0.
Output = 0110: O8 = 0, O12= 1, O14=0 &O9 = 0.
Output = 0011: O8 = 0, O12= 1, O14=0 & O13= 1.
Output = 0111: O8 = 0, O12= 1, O14=0 & O9= 1.
ForOutput = 1000: O8 = 0, O4= 0, O7=0& O6= 0.
Output = 1100: O8 = 0, O4= 1, O2= 0 & O3= 0.
Output = 1001:O8 = 0, O4= 0, O7=1 & O6= 1.
Output = 1101: O8 = 0, O4= 1, O2= 0 & O3= 1.
Output = 1010:O8 = 0, O4= 0, O6= 1 & O5= 0.
Output = 1110: O8 = 0, O4= 1, O2= 1 & O1= 0.
Output = 1011:O8 = 0, O4= 0, O6= 1 & O5= 1.

From the above expressions we can design a bit reference encoder by using one 2:1 MUX, one 4:1 MUX and one 8:1 MUX as shown in below schematic O8,

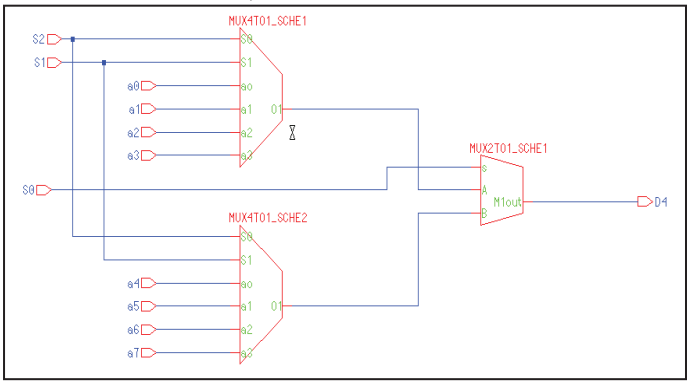


Fig. 8: Schematic of Bit Reference Encoder

O12 and O4 acts as selection lines as well as outputs of the flash ADC, remaining all outputs of comparators used as data inputs for MUXs used in encoder. By using this encoder along with 15 TMCCs, 4-bit Flash ADC is designed as shown in below fig. 9.

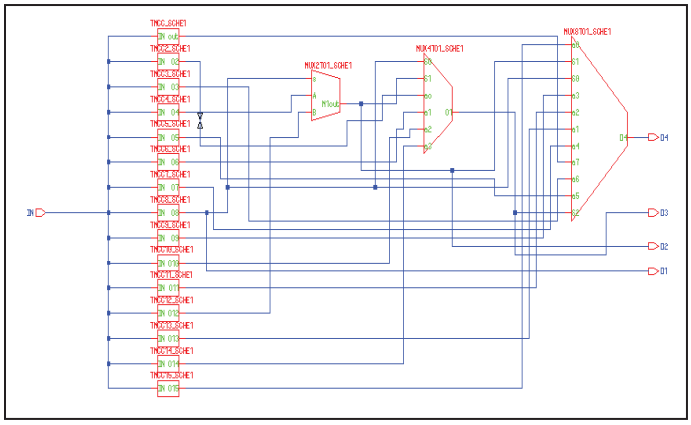


Fig. 9: Schematic of Flash ADC with TMCC and Bit Reference Encoder

The operation is same as for 3-bit flash ADC and resolution is difference. But now the 1.8V VDD is quantized into 15 different values each one have difference of 0.12v. This modified Flash ADC is simulated in 130 nm mentor graphics tool and the simulation waveform as shown below.

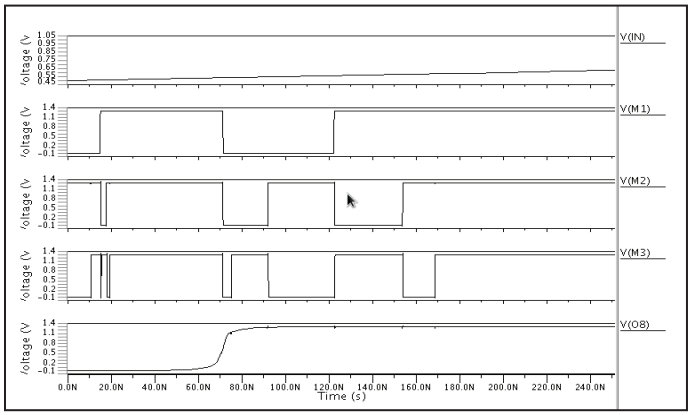


Fig. 10: Simulation Results of Flash ADC with TMCC and Bit Reference Encoder.

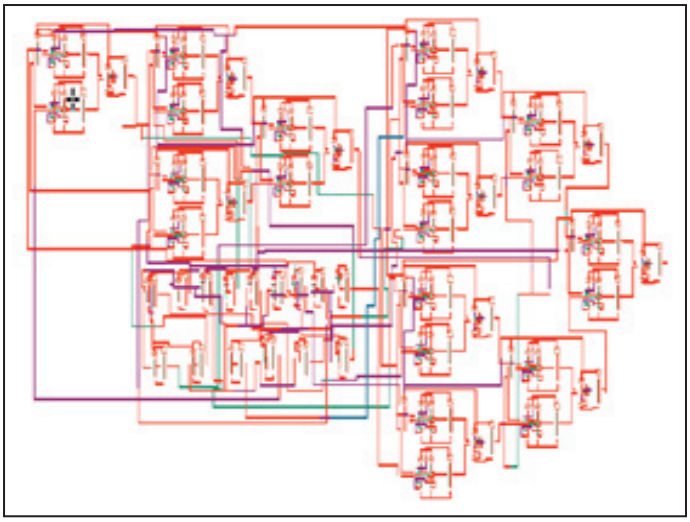

Fig. 11: Layout Diagram of Flash ADC with TMCC and Bit Reference Encoder

### C. Using TMCC and Gray to Binary Encoder

As earlier discussed flash type ADCs are have some drawbacks i.e. the Flash ADC using inverter based comparator suffers from the large area high power dissipation, and where as the Flash ADC with combination of the TMMCs and bit reference encoder is not suitable for high resolution ADCs is a chance of missing bits it leads to improper output as shown in fig. 12.

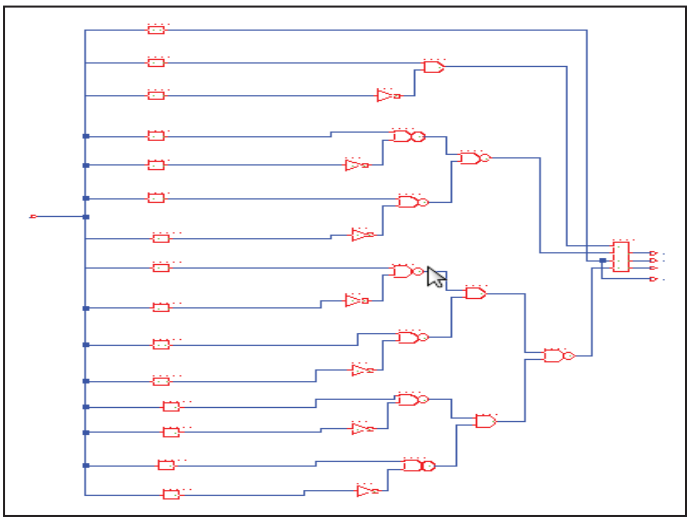

Fig. 12: Schematic Diagram of Proposed Flash ADC

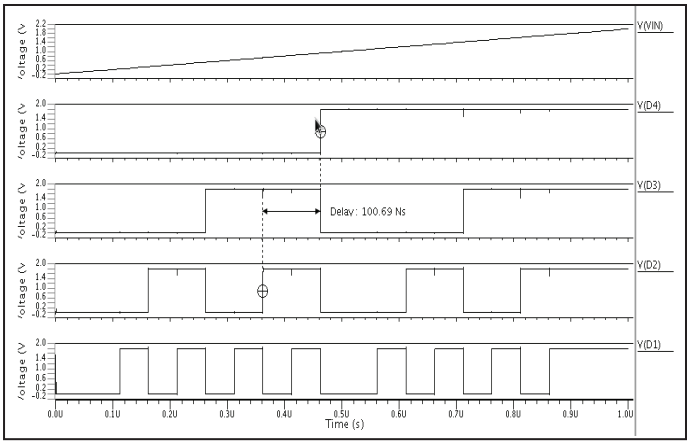


Fig. 13: Simulated Waveform of Proposed Flash ADC

To compensate the above mentioned drawbacks Flash ADC with TM Comparator Circuit and Gray to base2 encoder is proposed in this paper. The schematic for this proposed Flash ADC is shown in the fig. 12. It is constructed using TM Comparator Circuit and Gray to Base 2 encoder. This proposed ADC is simulated in Mentor Graphics tool in 130nm technology and its efficiency is calculated using results obtained from the simulated results shown in fig. 13.

After the simulation the layout of proposed ADC is laid out using pyxis assembly tool in mentor graphics.

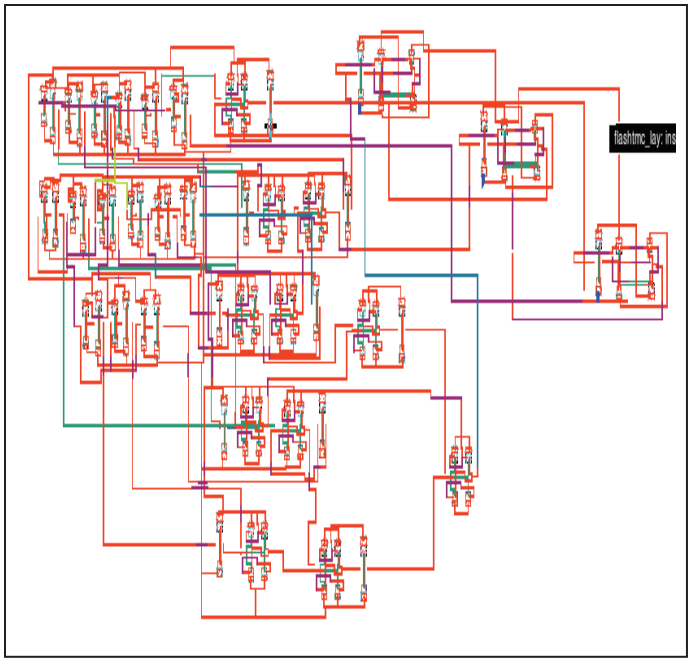

Fig. 14: Layout of the Proposed Flash ADC

After these simulation verifications some comparisons are made and tabulated for evaluating the efficiency of propped Flash ADC is shown in below Table 4.

Table 4: Comparison of proposed ADC with other ADCs

| Design specification | ADC [1] | ADC [2] | Extended ADC [2] | Proposed ADC |
|---|---|---|---|---|
| Architecture | Flash | Flash | Flash | Flash |
| Resolution | 3 bit | 3 bit | 4 bit | 4 bit |
| Supply voltage | 1.8v | 1.8v | 1.8v | 1.8v |
| Power dissipation | 3.22mw | 115.59nw | 128.59nw | 104.82nw |
| Area ($mm^2$) | 0.0105 | 0.0036 | 0.0051 | 0.0024 |
| technology | 130 | 130 | 130 | 130 |
| Missing bit | Nil | Nil | Nil | Nil |

## V. Conclusion

This proposed ADC is simulated in 130nm technology for efficiency evaluation in mentor graphics tool and finally found that this proposed ADC is area efficient and also power efficient.The main advantage of proposed ADC is low static power consumption because there is no resistor bank like conventional Flash ADC. The power dissipation of the proposed ADC is 35.65nw for input of 1.8v with 10MHz. in the development of high speed low power ADCs Aperture jitter, transistor matching, and increasing drain-bulk capacitance are the major problems, by using this proposed

ADC those problem can be reduces slightly and provide the low power and high speed flash ADC. In future we would like to test efficiency of this proposed ADC in coming technologies like 65nm and 32nm and also put effort to increase resolution and decrease the power dissipation.

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