FPGA Implementation of Algorithmic Counter Based Wallace Multiplier

[1]Sanjeeva Rao B, [2]Ram Kumar A
[1,2]Dept. of ECE, Sir.C.R.R College of Engineering, Eluru, India

Abstract

In this paper presents an algorithmic approach to construct high speed Wallace tree multiplier using proposed 7:3 counter along with full adder and half adder. This power efficient and high speed method can be used to implement counter based Wallace multiplier suitable for FPGA or ASIC synthesis tools. This concept is less complex as it avoids conventionally used multiplication and addition steps. It is an optimized method for Very Large Scale Integration (VLSI), applications.

Keywords

Wallace Multiplier, FPGA, ASIC, Counter Based Wallace, VLSI.

I. Introduction

Multiplication is basic and most widely used operation in digital systems. wallace tree multiplication improves the speed of this multiplication process. The operation of the Wallace tree multiplier is divided in three steps as shown in the fig. 1.

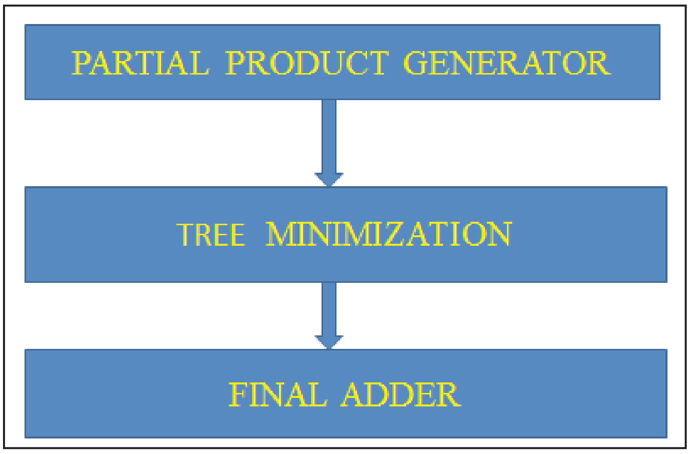


Fig. 1: Block Diagram of Tree Based Multiplication

After generating partial products, half adders and full adders are used for reduction of these partial products, until those are reduced to two rows. These two rows are finally added in final adder in order to get the result of the multiplication. A large number of papers have been published in the literature to improve the performance of the Wallace multiplier. A Booth-encoded based Wallace multiplier is proposed in [3] which uses Booth encoding to generate the partial products. In [4], a layout strategy is proposed to reduce the wiring delay of the tree reduction. This approach results in a slightly faster multiplier as compared to the Wallace multiplier. A number of architectures use high speed counters in Wallace tree reduction to reduce the delay of the partial product tree reduction. The architecture in [6] uses a technique similar to Wallace reduction [2] to compute the sum of N inputs where all the inputs have the same weight.The architecture computes the 1s in the columns by using only the full adders. A modified form of this architecture is presented in [7] which uses Ripple Carry Adders (RCAs) and FAs to perform the counting. This paper proposes a structural approach which can be used to implement the counter based Wallace multiplier. The proposed algorithm can be easily employed for the implementation of CBW multiplier of any size on FPGA and ASIC platforms.

The rest of the paper is organized as follows: Section II discusses the construction of the proposed Counter Based Wallace Multiplier (CBW). In Section III, simulation results of both traditional Wallace tree multiplier and proposed Counter Based Wallace Multiplier (CBW) are presented. The work is concluded in Section IV.

II. Counter Based Wallace Multiplier (CBW)

In this proposed Counter Based Wallace Multiplier (CBW),we use only a 7:3 counter along with half adders and full adders. We used the 7:3 counter proposed in [10] due to its simple and fast circuit. The boolean equations used to implement this counter is given as follows:

A. 7:3 Counter

The design of 7:3 counter is extensively studied in the literature and a number of architectures are proposed. The 7:3counter proposed in [10] is selected for the proposed CBWmultiplier due to its high speed operation. The Equation (1)gives the boolean functions for Sum, Cout1 and Cout2 for the 7:3 counter.

$$\text{Sum} = [(A \oplus B) \oplus (C \oplus D)] \oplus [(E \oplus F) \oplus G]$$
$$\text{Cout1} = (w1 \oplus w2) \oplus w3$$
$$\text{Cout2} = (w1.w2) + ((w1 \oplus w2).w3)$$

where

$$w1 = A.B + C.D + ((A + B).(C + D))$$
$$w2 = [((E + F).G + E.F)]$$
$$w3 = [A.B.C.D + ((A \oplus B)\ (C \oplus D))].[(E \oplus F) \oplus G]$$

The operation of counter based wallace multiplier is divided in three steps as shown in fig. 1.

For better understanding, this operation is simply explained using an 8-bit multiplication process.

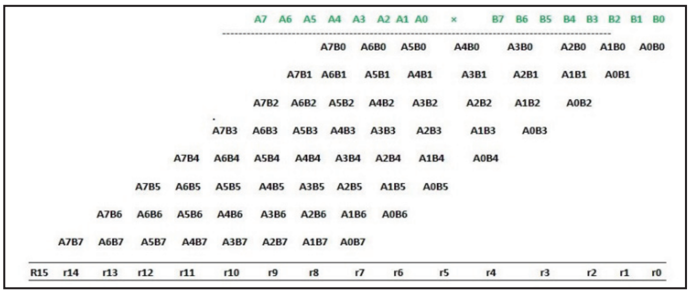
Step 1: Partial Product Generation

Let A and B are two 8 bit numbers .

A = [A7 A6 A5 A4 A3 A2 A1 A0]

B = [B7 B6 B5 B4 B3 B2 B1 B0]

The partial products for these two numbers as shown in following fig.



A7 A6 A5 A4 A3 A2 A1 A0 × B7 B6 B5 B4 B3 B2 B1 B0

								A7B0	A6B0	A5B0	A4B0	A3B0	A2B0	A1B0	A0B0
							A7B1	A6B1	A5B1	A4B1	A3B1	A2B1	A1B1	A0B1	
						A7B2	A6B2	A5B2	A4B2	A3B2	A2B2	A1B2	A0B2		
					A7B3	A6B3	A5B3	A4B3	A3B3	A2B3	A1B3	A0B3			
				A7B4	A6B4	A5B4	A4B4	A3B4	A2B4	A1B4	A0B4				
			A7B5	A6B5	A5B5	A4B5	A3B5	A2B5	A1B5	A0B5					
		A7B6	A6B6	A5B6	A4B6	A3B6	A2B6	A1B6	A0B6						
	A7B7	A6B7	A5B7	A4B7	A3B7	A2B7	A1B7	A0B7							
R15	r14	r13	r12	r11	r10	r9	r8	r7	r6	r5	r4	r3	r2	r1	r0

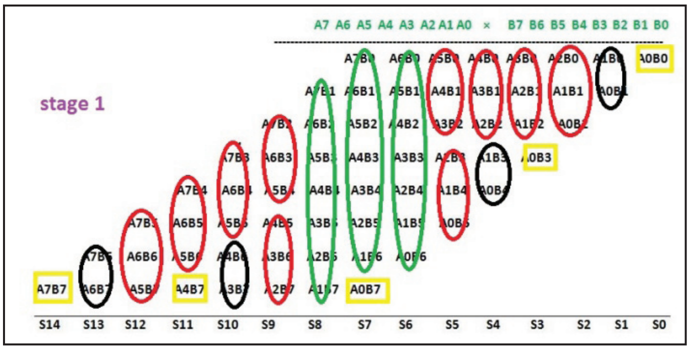

A7 A6 A5 A4 A3 A2 A1 A0 × B7 B6 B5 B4 B3 B2 B1 B0
stage 1
A7B0 A6B0 A5B0 A4B0 A3B0 A2B0 A1B0 A0B0
A7B1 A6B1 A5B1 A4B1 A3B1 A2B1 A1B1 A0B1
A7B2 A6B2 A5B2 A4B2 A3B2 A2B2 A1B2 A0B2
A7B3 A6B3 A5B3 A4B3 A3B3 A2B3 A1B3 A0B3
A7B4 A6B4 A5B4 A4B4 A3B4 A2B4 A1B4 A0B4
A7B5 A6B5 A5B5 A4B5 A3B5 A2B5 A1B5 A0B5
A7B6 A6B6 A5B6 A4B6 A3B6 A2B6 A1B6 A0B6
A7B7 A6B7 A5B7 A4B7 A3B7 A2B7 A1B7 A0B7
S14 S13 S12 S11 S10 S9 S8 S7 S6 S5 S4 S3 S2 S1 S0

Fig. 2: Partial Product Generation and Reduction of Stage 1

Step 2: Reduction of Partial Products

For reduction of partial products, in this approach, we use a 7:3 counter along with half adders and full adders. In stage 1, as shown in fig, combinations are made for reduction of computations, using a 7:3 counter along with half adders and full adders.

In stage 2, we have four rows, which are obtained from the reduction of the partial products of the eight rows.it is illustrated in fig. The reduction is from four rows to three rows, in stage 3. At this stage ,these three rows are minimized to two rows using full adder and half adders.

Step 3: Final Adder

Now, those two rows are added to obtain the final result.
In this way, we can construct, any size of multiplication using this proposed algorithmic approach.

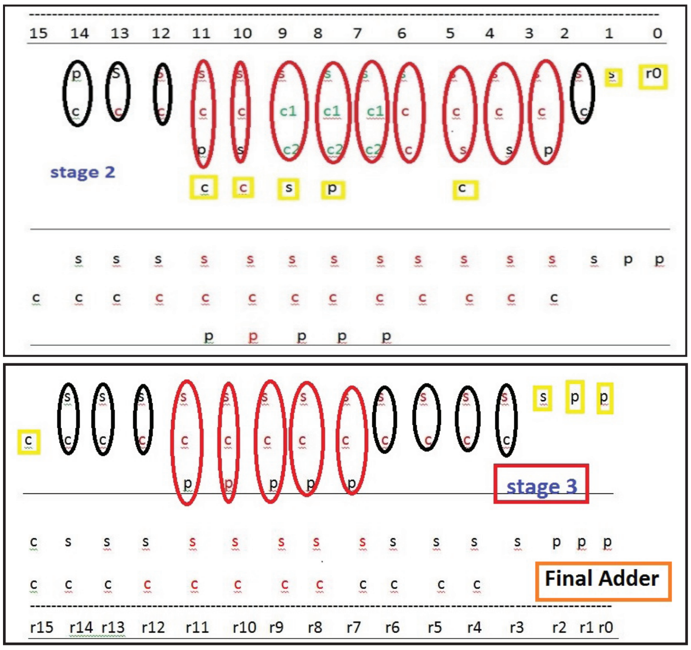


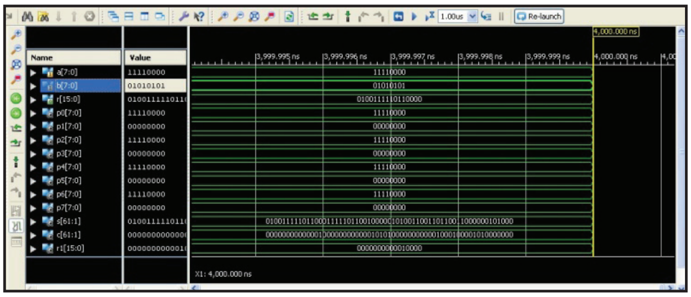
Fig. 3: Tree Minimization of Stage 2, Stage 3 and Final Addition

III. Simulation Results

Both traditional Wallace and counter based Wallace multipliers are compared in this section. Simulation wave forms of traditional Wallace and counter based Wallace multipliers are separately illustrated in following, fig. 4 and fig. 5.

The internal computational stages are compared for 8-bit, 16-bit, 32-bit, 64-bit, 128-bit and 256-bit and summarized in Table 1'

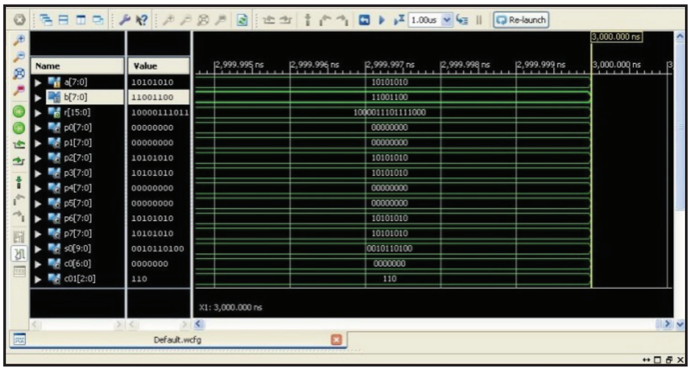
Maximum combinational path delay: 11.719ns
(5.517nslogic, 6.202ns route)(47.1% logic, 52.9% route)
Maximum combinational path delay: 11.138ns.
(5.274ns logic, 5.864ns route)47.4% logic, 52.6% route).



Name	Value
a[7:0]	11110000
b[7:0]	01010101
r[15:0]	0100111110110000
p0[7:0]	11110000
p1[7:0]	00000000
p2[7:0]	11110000
p3[7:0]	00000000
p4[7:0]	11110000
p5[7:0]	00000000
p6[7:0]	11110000
p7[7:0]	00000000
s[61:1]	0100111110110001111101100100000101001100110110011000000101000
c[61:1]	0000000000000100000000000010101000000000000100010000101000000000
r1[15:0]	0000000000010000

X1: 4,000.000 ns

Fig. 4: Simulation Waveform for Wallace Multiplier



Name	Value
a[7:0]	10101010
b[7:0]	11001100
r[15:0]	1000011101111000
p0[7:0]	00000000
p1[7:0]	00000000
p2[7:0]	10101010
p3[7:0]	10101010
p4[7:0]	00000000
p5[7:0]	00000000
p6[7:0]	10101010
p7[7:0]	10101010
s0[9:0]	0010110100
c0[6:0]	0000000
c01[2:0]	110

X1: 3,000.000 ns

Fig. 5: Simulation Waveform for Counter Based Wallace Multiplier

For an 8-bit counter based Wallace multiplication, it is already shown in section II, that it require only three stages.
Both the multipliers are implemented using the XILINX version 10.1 and simulated using MODELSIM simulator.

Table 1: Comparison of Reduction Stages

Size	Number of stages of traditional Wallace multiplier	Number of stages of counter based Wallace multiplier
8-bit	4	3
16-bit	6	4
32-bit	8	4
64-bit	10	5
128-bit	11	6
256-bit	13	7

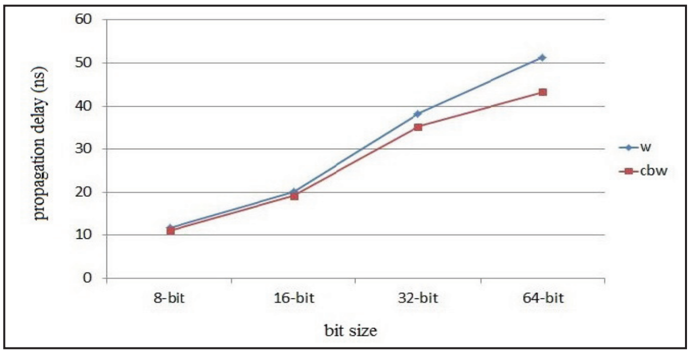


Fig. 6: Comparision Graph

IV. Conclusion

In this paper, power efficient and high speed counter based Wallace multiplication was discussed. This approach can be used to construct and implement any size of multiplication on FPGA as well as ASIC. In this approach we have used a 7:3 counter along with full adder and half adder. It is most suitable high speed applications. All the simulated waveforms are discussed.

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Sanjeeva Rao B received his B.Tech Degree in Electronics and Communications Engineering from Akula Gopayya College of Engineering and Technology, Tadepalligudem, India in 2012. At present, he pursuing M.Tech Degree in VLSI in Sir CRR College of Engineering, Eluru, India. His area of interests including low power VLSI design, Electronic measurement Techniques, Microcontrollers and Embedded Systems Design.

Ram Kumar A received his B.Tech degree in Electronics and Communications Engineering and M.Tech degree in VLSI systems design from Swarnandhra College of Engineering and Technology, Narsapur, India in 2007 and 2012 respectively. At present, he is an Assistant Professor in Dept. of ECE in Sir CRR college of engineering, Eluru, India. His research interests include digital signal processing and digital VLSI.