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Glitch Energy Reduction and SFDR Enhancement Techniques for Segmented Current Steering DAC

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Abstract

In communication and video systems, Current-steering Digital-to-Analog Converters (DACs) perform an important role as they have the benefits of speed, linearity, and power efficiency. The Glitch is an important measure which is to be considered in the quality of output signal. This project proposes a glitch reduction approach by the combination of Dynamic Capacitance Compensation (DCC) and Grouped Random Rotation Thermometer Code (GRTC) for segmented current switches in a current-steering Digital-to-Analog Converter (DAC). The method was proved successfully by a 10-bit 500 MHz segmented current steering DAC with a power consumption of 31.6 mW. During major carry transitions at output, the experiment results yield very low-glitch energy of 0.6 pVs.

Keywords

Segmented, Current Switch, Digital to Analog Converter (DAC), Dynamic Capacitance, GRTC, Glitch Energy

I. Introduction

All real world Analog signals such as voice, temperature are generally changed into digital form, which can be accessed very easily in present digitized systems. In almost all modern machines, the digitized data should be converted back into the Analog data in order to make some real world applications. The device which does this work is digital to Analog converter. Complex fewer components such as switches resistor elements and current sources can perform this conversion and the outputs of those can be used to drive devices such as mechanical servos, loudspeaker, and video displays etc. DAC's are involved in digital systems in which Analog signal is made into digital form by Analog to digital converters, and then again reconverted into Analog form by using DAC.

Current steering digital to analog converters can be implemented in 3 different architectures known as unary, binary and segmented architectures. The weights of all current sources used in unary architecture are equal and thermometer decoder is used in order to select current sources. The weights of current sources used in binary weighted depend on the position of the current source and no decoder is used here to select current source. Segmented architecture includes unary at MSB side and binary at LSB side Keeping in mind for power consumption, chip size and complexity of the circuit, the binary weighted architecture is selected as best suitable for medium-to-high resolution and sampling rate. The approach followed here can be used in the LSB part of the segmented architecture. When the binary-weighted current-steering DAC tends to operates at a high sampling rate, glitch caused because of the transitions of current switches will have considerable impact on the output signal. Glitch is one of the major parameter which degrades the performance of the DAC. As these current steering DAC's perform major role in the video systems, these glitches at the output may produce the colour shifts at the borders on the screen when glitch produced is higher. As a result, the Spurious Free Dynamic Range (SFDR) gets decreased as the amplitude of the glitch increases. The glitch with major amplitude occurs when all the bits at the input are changed once at a time as shown in fig. 1. The timing skews occur among various current sources because of mismatches among various switches.

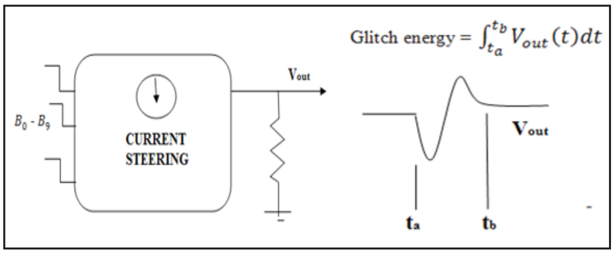


Fig. 1: Glitch During All Bit Transition

The glitch energy is generally known as the time integral of the analog value of the transient glitch. Even though the deglitching techniques namely, return to zero (RZ) [6] and quad switching [7] helps to reduce the glitches, the main disadvantage of quad switching is, dynamic power consumption and complexity tends to increase, where as the RZ technique generally not used in many applications. A recent technique of dynamic capacitance compensation [1] along with grouped random rotation thermometer code (GRTC) technique is used to reduce the glitch in the output of a DAC.

In this brief, a 10 bit 500-MHz segmented current steering DAC with less number of buffers and retiming latches. Dynamic compensation capacitance was used to reduce the glitches because of different timing skews and GRTC technique is used to reduce the mismatches among different current switches.

II. Overall Architecture

Fig. 2 gives the functional diagram of the proposed 10 bit binary weighted current steering digital to analog convertor. Here B0-B9 is the digital input bits at the buffers which have been given from the 10 bit asynchronous counter. The input buffers used here are inverter based buffers which eliminate the transient noise is shown in fig. 3. D latch is a retiming latch constructed using SR gated latch which is shown in fig. 4.

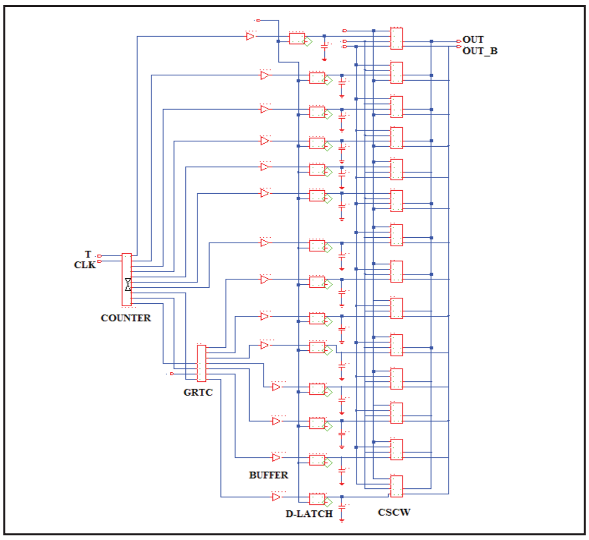


Fig. 2: Function Diagram of Proposed DAC

In order to reduce the power dissipation and area, the number of buffers and latches used are linearized. Here only single latch and buffer are used for seven lower LSB bits, two latches and two buffers are used for bit 8 and finally four latches and four buffers are used for last MSB bit due to the increase in the loading. The overall latches used here are 14, which is very less in number while compared with the unary structure (1023 are needed). As a result, the binary structure reduces the complexity when compared to unary architecture.

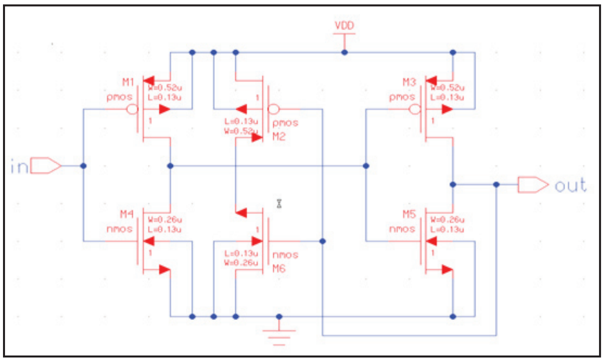


Fig. 3: Schematic of Buffer

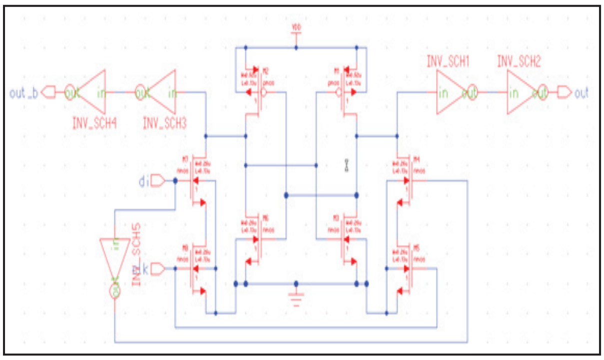


Fig. 4: Schematic of D-latch

The current steering DAC replaces the resistor element with a MOSFET switch which effectively reduces the area of entire DAC. The schematic of combined current source and switch is shown in fig. 5. The CSCW cell joins the current source and current switch in order to minimize the parasitic capacitance. The dynamic compensation capacitance circuit which is used to minimize the timing skews is placed between d-latch and CSCW.

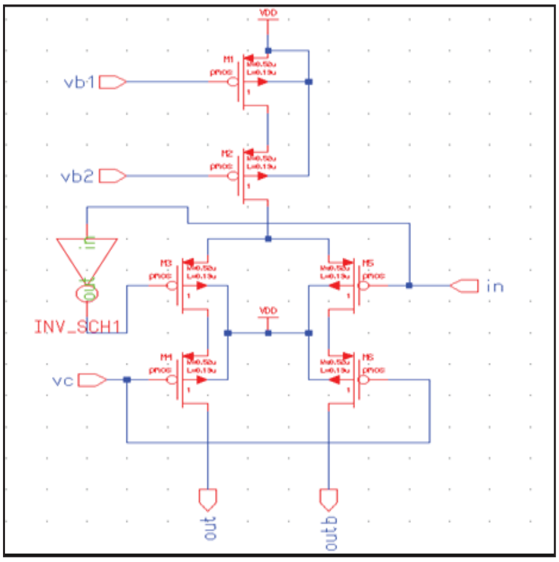


Fig. 5: Schematic of CSCW Cell

III. Operation and Circuit Implementation of GRTC

Grouped Random Rotation Thermometer Code (GRTC) is a Dynamic Element Matching (DEM) technique [2] used to minimize the mismatches among different loadings of current sources. Here the concept of equalizing weights is used in which the total number of current sources is made into two equal groups such that the total weights of currents coming from each individual group are equal, this generates no offset voltage error after the process of randomization. As a result the performance of the overall DAC structure tends to increase. In GRTC technique the randomness of the GRTC tends to depend on the randomness of the Pseudo Random Number Generator (PRNG) which is an internal circuit used in GRTC. The GRTC technique effectively performs the DEM by randomly rotating the current sources. Clear information of both conventional thermometer and GRTC is shown in fig. 6.

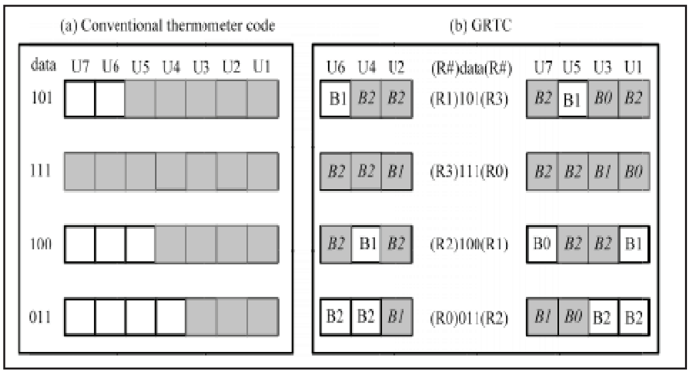


Fig. 6: Variation Among Thermometer Code and GRTC

In conventional technique the number of current sources selected depends on the input bit code, but in this technique the number of current sources that should be on depends on the randomness of the PRNG. R# on the right and left of a particular binary data represents the number of right circular rotation to be made. The detailed implementation of 3 bit GRTC structure which has been used in this proposed paper is given in figure below. The seven outputs of GRTC circuit are assigned to seven current sources with same weight of current.

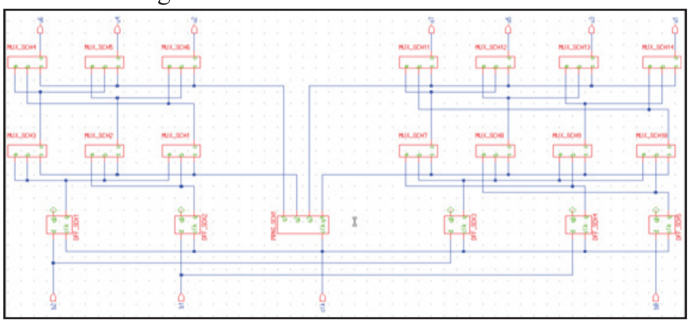


Fig. 7: Schematic of 3 Bit GRTC

IV. Circuit Design and Analysis

As shown in fig. 2, the output signals from the latches will definitely have timing skews due to different loadings. In order to minimize the timing skew, first we analyze various loading effects strictly of retiming latches. To make sure that the retiming latch can operate at 500 MHz successfully, we must minimize the input capacitance of a CSCW to be less than 600 femto farad. Knowing the performance of d-latch for different CL values, the rise time for the output of retiming latch is 76ps for CL value of 50 femto farad, and 500 ps for the CL value of 600 femto farad. On the other hand increasing the value of CL increases the rise time and also decreases the slew rate, slowing the slew rate reduces the glitch at the output of DAC. As a result the selection of value of CL plays an important role. The dynamic input capacitance (Incap) is both frequency and bias dependent. Where I(vin) is ac current of the current source,

Incap = -Im(I_{ac})/(2πf x v_{ac}) = I(vin) / (2πf x1v)

The dynamic capacitance values for different switches are analyzed and are given in the table below in units of femto farad with three different compensations.

Table 1: Dynamic Capacitance Values of Current Switches

Current switch	Without compensation (fF)	Full compensation (fF)	Partial compensation (fF)
S0	Cu	128Cu	32Cu
S1	2Cu	128Cu	32Cu
S2	4Cu	128Cu	32Cu
S3	8Cu	128Cu	32Cu
S4	16Cu	128Cu	64Cu
S5	32Cu	128Cu	64Cu
S6	64Cu	128Cu	128Cu
S7	128Cu	128Cu	128Cu
S8_1,S8_2	128Cu	128Cu	128Cu
S9_1,S9_2, S9_3,S9_4	128Cu	128Cu	128Cu

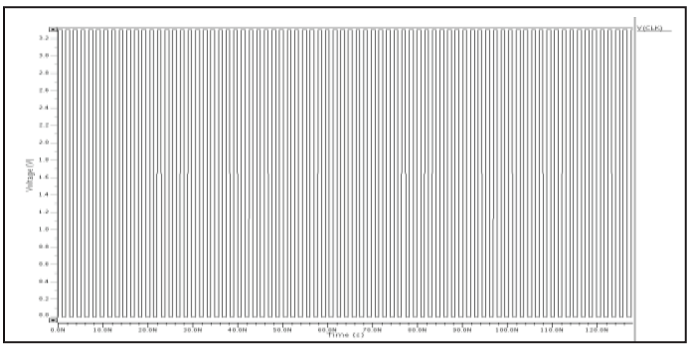
Three different conditions analyzed here are: (1) without compensation, (2) with full compensation and (3) partial compensation. Particularly for full compensation all capacitance values taken are 128Cu, where 1 Cu equals to 1.8 femto farad. During partial compensation current switches S0-S3 is compensated to 32Cu, S4-S5 is compensated to 64Cu and remaining switches are compensated to 128Cu. Through the comparison of these different compensations it is known that power, area and speed of partial compensation are very much better than remaining two. Output impedance of a current switch is the major parameter which decides integral non linearity error (INL) and Spurious Free Dynamic Range (SFDR) given below.

$$\text{INL (LSB)} = \frac{R_L 2^{2N}}{4Z_0}$$

$$\text{SFDR} \sim 20\log(2^N/INL)$$

V. Results of Experiment

As the proposed DAC is running at 500 MHz sampling rate, the time period of 1 clock signal is 2 ns. So that entire analog output can be obtained by 2048 ns. The clock and the analog output for the 10-bit digital input from 0000000000 to 1111111111 are shown below.



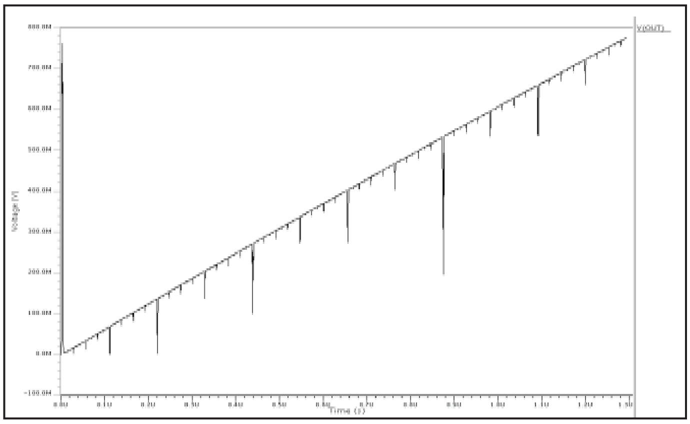


Fig. 8: Analog Output of a Proposed DAC for 500 MHz

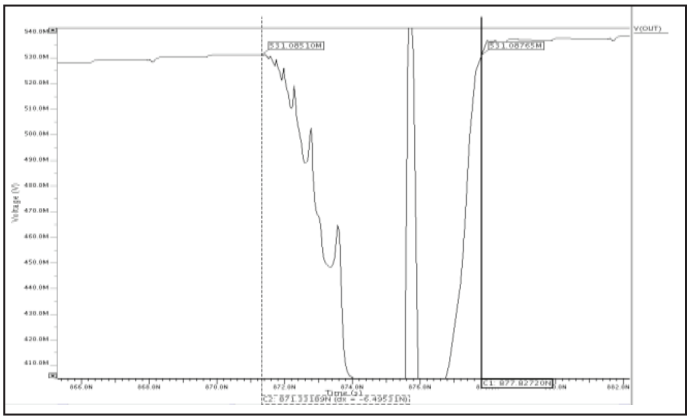


Fig. 9: Glitch During Major Transition

Table below shows the comparison of various parameters of proposed DAC with remaining other papers.

Table 2: Performance Summary and Comparisons

	This work	[1]	[5]	[8]
Technology	0.13µm	0.18µm	0.35µm	0.18µm
Resolution	10	10	12	10
Sample rate (MS/s)	500	400	120	250
Best SFDR (DB)	60	58	71	60
Glitch Energy (pV)	0.6	1	31	2.64
Supply voltage (V)	3.3	1.8	3	1.8
Power consumption (mW)	31.6	20.7	52.5	22
FOM1 (10^9)	16202	19787	9362	11636
FOM2 (10^9)	4531	5293	390	5818

The proposed DAC has better sampling frequency and better reduced glitch energy when compared with remaining [1], [5] and [8].

VI. Conclusion

This brief proposes an architecture of 10 bit 500-MS/s segmented current steering DAC which includes both Dynamic Capacitance Compensation (DCC) and Grouped Random Rotation Thermometer (GRTC) code techniques. These two techniques reduce the glitch energy of an output signal of DAC to a far extent which in turn improves SFDR. This experiment results low glitch at high output frequency. The amount of glitch energy obtained during major carry transition is only 0.6 pVs. The DAC is implemented using 0.13 µm CMOS technology consumes 31.6 mW at 500 MHz clock rate. In addition, the GRTC also expands the range of single-segment binary to thermometer code decoder, simplifies the design and reduces the active area of the DAC.

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