Future Challenge in Chip Technology 2015 Onwards

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Abstract
Each year, technology brings a wealth of advancement that could alter the future. Many of them are a long way from being viable, and some may never come to fruition, but the mere fact that each day is another chance for the world to solve the fossil fuel crisis, or cure cancer, is inspiring .In this paper Discussion of the Moore's law in current era and for the future will be done. Discussing and challenging the technology in terms of gate length, mask marking, fab flow and variation, patterning, interconnects, etching the surface, atomic-level scaling, plasma methods etc.

Keywords
Moore's Law, Etching, Atomic level scaling , Super Computing, chip, smart phones, nanometers, transistors, node, designs, r&d.

I. Introduction
Technology is following to Moore's law since 50 years (Fig. 1), [2]. The number of transistors on a computer chip would double every year. This doubling has enabled Smartphone and tablet technology that has revolutionized computing, but continuing the pattern will come with high costs [1] but according to this, we are going for 5nm in coming next 7-8 years. If the technology reaches at this point then Moore's law may be partially/totally changed due to technical limit.

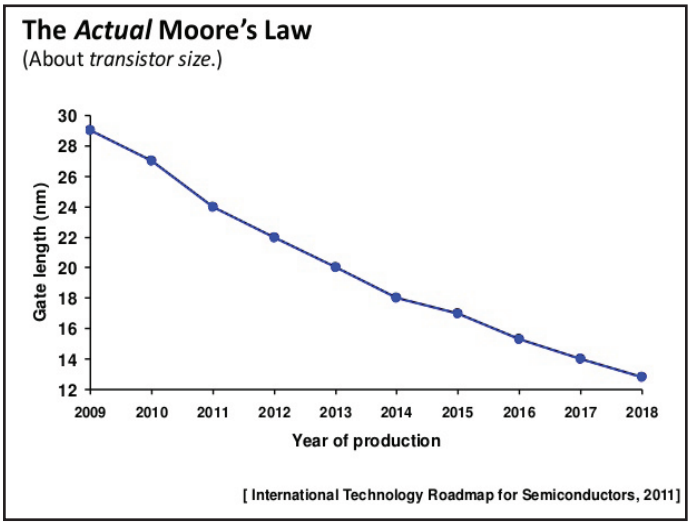

Fig. 1:

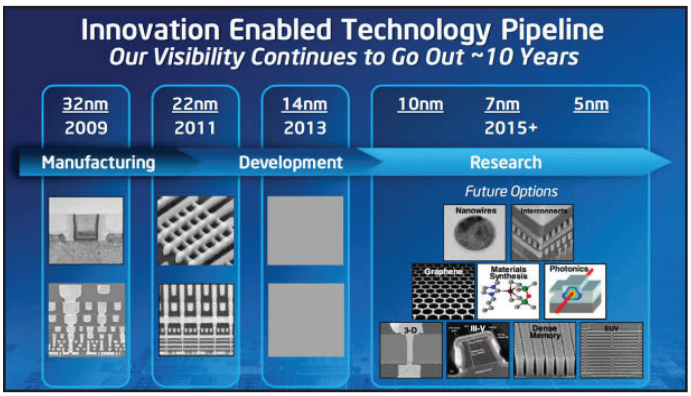

Fig. 2:

II. Summary and Discussion
The following picture shows the difference that 128 MB scandisk in 2005 and 128 GB scandisk in 2014 in same size. It is difference in only 9 years. (Fig. 3)

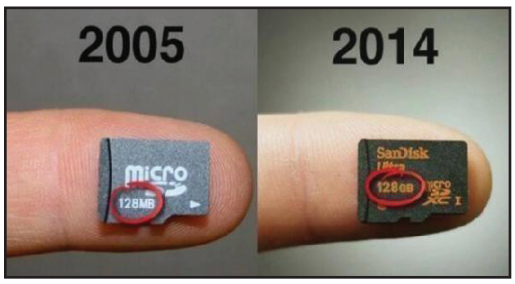

Fig. 3:

Researcher has various opinions regarding Moore's law. According to "The Economist", various researches how their predictions for the ending of Moore's law up to 2025 or behind that due to technical limits. (Fig. 4-5)

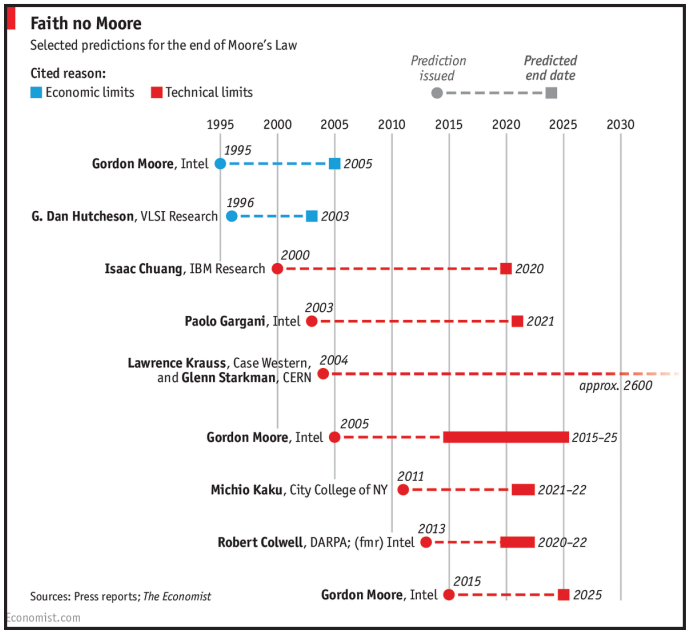

Fig. 4:

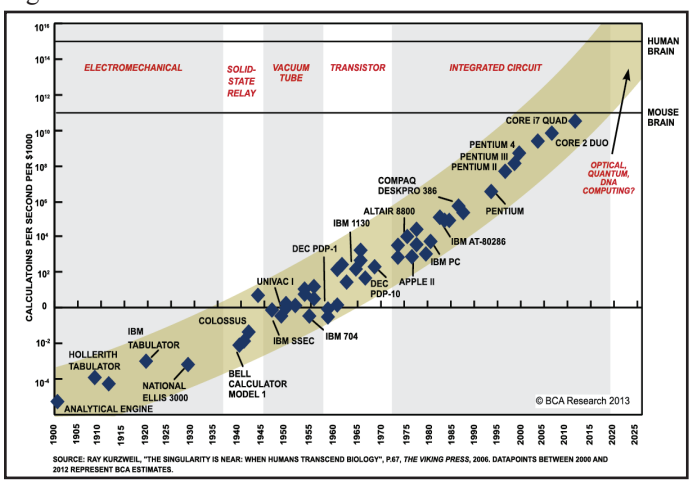

Fig. 5:

According to mark Lapedus, a Fabrication challenge may have been started behind 10nm in 2015 onwards [2]. To achieving this target, we require the new technology, in which everything may be in new concept like Photo mask designing, Lithography, flow changes, power of plasma, biasing voltage, Plasma Technology [3,4,5,6] etching equipment etc.

But in present era, The mask shapes got smaller and more complex as we went to 14nm and it will continue to get smaller and even more complex at 10nm. Extreme Ultraviolet (EUV) lithography missed the market window at 10nm. So, chipmakers will extend 193nm lithography and multiple patterning to 10nm. Optical Proximity Correction (OPC), is used to modify the mask patterns to improve the printability on the wafer. OPC makes use of assist features, which are getting smaller and more complex at each node. Obviously, the process steps become more complex at each node. If you look at the cost and technical challenges associated with scaling, it's very high. There are problems as you go to 10nm and below. You have to manipulate things at the atomic level. The interfaces become more critical. In this pipeline, the Lithography is still the biggest challenge and most expensive step, in the fabrication. The migration towards finFETs and other devices at the 20nm node and beyond will require a new array of chip-manufacturing technologies. Multiple patterning, hybrid metrology and newfangled interconnect schemes are just a few of the technologies required for future scaling. In addition, the industry also will require new techniques that can process structures at the atomic level. For example, a transistor gate width could consist of only 20 atoms at the 7nm node, compared to 140 atoms at 20nm. So, to help manipulate the atoms in future devices, chipmakers will likely require a new and disruptive technology called atomic layer etch. Atomic layer etch, sometimes known as ALE, is a next-generation plasma etch technology that enables layer-by-layer, or atom-by-atom, etching for IC designs. ALE is also related to Atomic Layer Deposition (ALD). ALD has been in IC production for years, but ALE has been a solution looking for a problem and stuck in R&D labs for nearly two decades. Plasma Etching, the process step that removes materials from the wafer to create the features of a device, is a critical but somewhat unheralded tool in the fabrication. Going forward, etch is becoming more important in the flow. For example, extreme ultraviolet (EUV) lithography remains delayed, forcing chipmakers to deploy multiple patterning techniques starting at 20nm. For decades, meanwhile, chipmakers have used the same basic plasma etcher, sometimes called Reactive Ion Etch (RIE), in the fab. In general, the etcher is used for two main and separate applications—conductor and dielectric. Conductor etch helps shape the active materials, while dielectric etch carves patterns in insulating materials to create barriers. In RIE, a tool combines many gases in the reactor at the same time. Basically, ALE also provides conductor and dielectric etch, but the newfangled technology handles these functions at a finer scale or at the atomic level. And unlike RIE, ALE performs single unit steps to achieve set outcomes, which may impact the overall throughput of the process. So for atomic-level scaling, the next-generation etch solution is clear—AIL. The big question is what can ALE do in the fab and will it achieve the same success as ALD. The different dry equipment approaches to atomic layer etching (ALEt) are reviewed. Now, According to future, it seems that DNA computer is future. In search of a more affordable way forward, scientists are exploring the use of DNA for its programmability, fast processing speeds and tiny size. So far, they have been able to store and process information with the genetic material and perform basic computing tasks. To making DNA computer, Technology may face the challenge to replace conventional silicon microprocessor. This is based on human DNA. Due to this, Moore's law may be out dated in future if technology reaches their limits.

To maintain the Moore's law, we must think in new direction with new technology.

III. Future Scope

Here we conclude that the past 20 years were truly the great old days for Moore's Law scaling and microprocessor performance; dramatic improvements in transistor density, speed, and energy, combined with micro architecture and memory-hierarchy techniques delivered 1,000-fold microprocessor performance improvement. The next 20 years—the pretty good new days, as progress continues—will be more difficult, with Moore's Law scaling producing continuing improvement in transistor density but comparatively little improvement in transistor speed and energy. As a result, the frequency of operation will increase slowly. Energy will be the key limiter of performance, forcing processor designs to use large-scale parallelism with heterogeneous cores, or a few large cores and a large number of small cores operating at low frequency and low voltage, near threshold. Aggressive use of customized accelerators will yield the highest performance and greatest energy efficiency on many applications. Efficient data orchestration will increasingly be critical, evolving to more efficient memory hierarchies and new types of interconnect tailored for locality and that depend on sophisticated software to place computation and data so as to minimize data movement. The objective is ultimately the purest form of energy-proportional computing at the lowest-possible levels of energy. Heterogeneity in compute and communication hardware will be essential to optimize for performance for energy-proportional computing and coping with variability. Finally, programming systems will have to comprehend these restrictions and provide tools and environments to harvest the performance. The past 20 years were truly the great old days for Moore's Law scaling and microprocessor performance; dramatic improvements in transistor density, speed, and energy, combined with micro architecture and memory-hierarchy techniques delivered 1,000-fold microprocessor performance improvement. The next 20 years—the pretty good new days, as progress continues—will be more difficult, with Moore's Law scaling producing continuing improvement in transistor density but comparatively little improvement in transistor speed and energy. As a result, the frequency of operation will increase slowly. Energy will be the key limiter of performance, forcing processor designs to use large-scale parallelism with heterogeneous cores, or a few large cores and a large number of small cores operating at low frequency and low voltage, near threshold. Aggressive use of customized accelerators will yield the highest performance and greatest energy efficiency on many applications. Efficient data orchestration will increasingly be critical, evolving to more efficient memory hierarchies and new types of interconnect tailored for locality and that depend on sophisticated software to place computation and data so as to minimize data movement. The objective is ultimately the purest form of energy-proportional computing at the lowest-possible levels of energy. Heterogeneity in compute and communication hardware will be essential to optimize for performance for energy-proportional computing and coping with variability. Finally, programming systems will have to comprehend these restrictions and provide tools and environments to harvest the performance.

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