

FPGA Implementation of LTE-Advanced Downlink Physical Layer Transceiver

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Abstract

To achieve a higher bit rates up to 1 Gbps for meeting the growing needs of the users of the mobile communication system the 3rd Generation Partnership Project (3GPP) introduced the Long Term Evolution Advanced (LTE-A) as an advanced standard for the mobile communication systems. The new features added by the LTE-A on the physical layer is a direct consequence for applying new modulation and coding techniques for both the Uplink and Downlink. The Orthogonal Frequency Division Multiple Access (OFDMA) was applied for the Downlink and the Single Carrier Frequency Division Multiple Access (SC-FDMA) was applied for the Uplink as well as turbo coding. This paper presents the design and implementation of the LTE-A downlink transmitter and receiver using a Field Programmable Gate Array (FPGA) according to release 10/11 on Virtex 6 XC6VLX240T FPGA kit using Xilinx® ISE® Design Suite version 13.3. All stages of the LTE-A downlink physical layer (PHY) transceiver, besides the time and frequency synchronization in a receiver, are implemented with 2x2 MIMO and Intra-band contiguous Carrier Aggregation type with two Component Carriers.

Keywords

LTE, 4G, 3GPP, OFDM, LTE-advanced downlink physical layer, release 10, release 11, Xilinx Design Suite, virtex 6 XC6VLX240T FPGA.

I. Introduction

The 3GPP has introduced the complete specifications of LTE-A to meet the growing needs to higher data rates in mobile communication systems. LTE Release 8 can provide up to 50 Mbps for uplink and 100 Mbps for downlink, while LTE-A, starting from Release 10, can provide up to 1 Gbps as peak data rates for downlink, as well as higher throughput, higher coverage, and lower latencies [1-9]. LTE and LTE-A have a scalable bandwidth of 1.4, 3, 5, 10, 15 or 20 MHz. The LTE-A PHY is a highly efficient facility for conveying both data and control information between an enhanced base station (eNodeB) and mobile User Equipment (UE). OFDMA is utilized in LTE-A downlink PHY while SC-FDMA is used in the uplink [10].

For higher data rates, the LTE-A should support Carrier Aggregation (CA) that act as a solution to bandwidth extension for large transmission bandwidths from 40 MHz to 100MHz and high peak data rate of 500 Mbps in the uplink and 1Gbps in the downlink [11-14]. There are three Carrier Aggregation scenarios; which are Intra-band contiguous, Intra-band non-contiguous and Inter-band non-contiguous Carrier Aggregation. The Intra-band contiguous uses a single frequency band and is the simplest form of CA from the implementation point of view while the Intra-band non-contiguous is aggregate, not adjacent multi-carriers, then two transceivers may be required. This adds a significant complexity to the UE, an increase the amount of power consumption and an increase in the cost. The Inter-band non-contiguous type uses different frequency bands. That is why the UE may have to use multiple transceivers. So, the cost, performance and power consumption are affected

considerably. On the other side it can improve the system mobility by exploiting the radio propagation characteristics of different bands [15-18]. Also, LTE-A supports the Multipoint Transmission and Reception as Multi Input Multi Output (MIMO) that ensure more system throughput. The MIMO systems can achieve significant higher data rates more than the traditional single-input, single-output (SISO) channels [19-20]. This paper presents the design and implementation of the LTE-A downlink PHY transceiver. The design is based on 2x2 MIMO and Intra-band contiguous CA type with two Component Carriers (CCs). The implementation is done using FPGA on Virtex 6 XC6VLX240T FPGA kit according to release 10 using Xilinx package version 13.3. The implementation of every stage in both the transmitter and receiver is verified.

The paper is organized such that: section two presents the design and implementation of the LTE-A transmitter and receiver building blocks. Section III introduces the full system verification while the full system and its area optimization strategy utilization on the Xilinx Vertix 6 are described in section four and the carrier aggregation scenario in section five.

II. LTE-Advanced Transmitter and Reciver Implementation

The implementation of LTE-advanced in this paper is built according to release 10 specifications with Frequency Division Duplex (FDD) frame structure. The bandwidth of the implemented system is 3 MHz, the number of sub-channels is 15, the number of sub-carrier is 180, the Inverse Fast Fourier Transform (IFFT) and the Fast Fourier Transform (FFT) size are 256, the rate of turbo encoder/decoder is 1/3, and the system input data is one OFDM symbol with length 96 bits [21]. The implemented transmitter and receiver block diagrams are shown in Figure 1 and Figure 2 respectively. In the following sections, all the building blocks in the transmitter are implemented with the FPGA and their reverse operations are done in the receiver. Finally, the overall system verification (transmitter/receiver) was done.

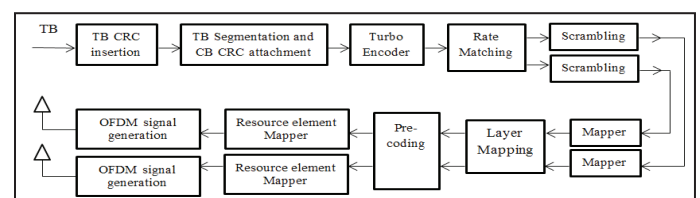


Fig. 1: The Block Diagram of the LTE-Advanced Downlink Physical Layer Transmitter [21].

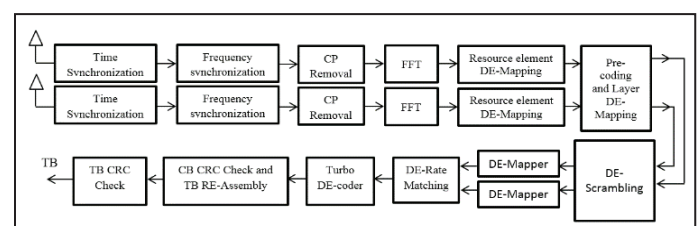


Fig. 2: The Block Diagram of the LTE- Advanced Downlink Physical Layer Receiver [21].

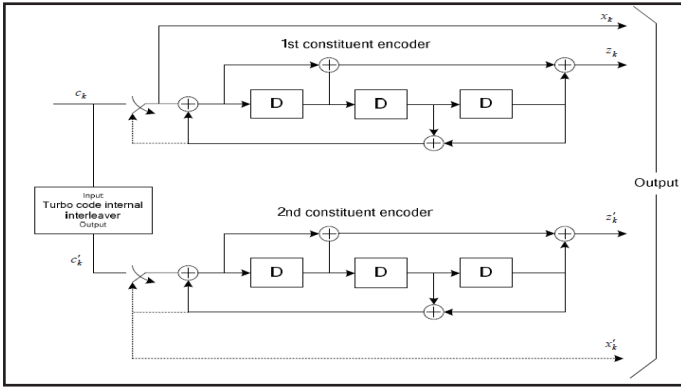


Fig. 7: Structure of Rate 1/3 Turbo Encoder [22].

The output of the Segmentation block is applied to the input of the Turbo Encoder block. Fig. 8 shows the implementation testing results of the Turbo Encoder block. It shows the encoder input data and the three parallel output sequences (systematic, parity_1 and parity_2) that was calculated according to the following equations [22]:

$$d_k^{(0)} = x_K, d_{K+1}^{(0)} = z_{K+1}, d_{K+2}^{(0)} = x'_K, d_{K+3}^{(0)} = z'_{K+1}$$

$$d_k^{(1)} = z_K, d_{K+1}^{(1)} = x_{K+2}, d_{K+2}^{(1)} = z'_K, d_{K+3}^{(1)} = x'_{K+2}$$

$$d_k^{(2)} = x_{K+1}, d_{K+1}^{(2)} = z_{K+2}, d_{K+2}^{(2)} = x'_{K+1}, d_{K+3}^{(2)} = z'_{K+2}$$

Where K is the number of input bits.

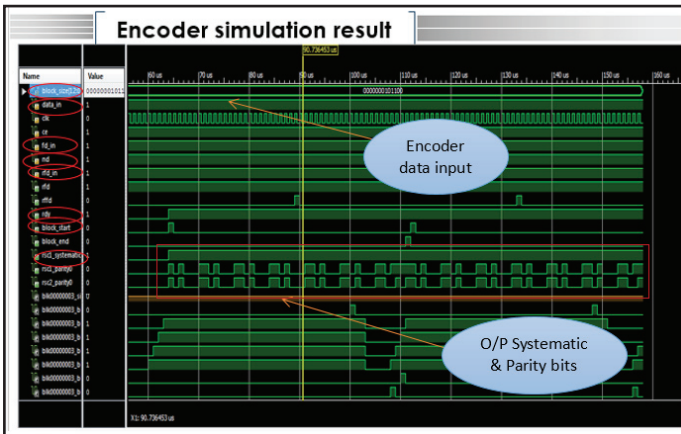


Fig. 8: The Testing Results of the Turbo Encoder

2. The Turbo Decoder

The Turbo Decoder do the reverse operation of the Turbo Encoder. Fig. 9 shows The Turbo Decoder implementation testing results, where it shows the three parallel input sequences (systematic, parity_1 and parity_2) and the output data sequence.

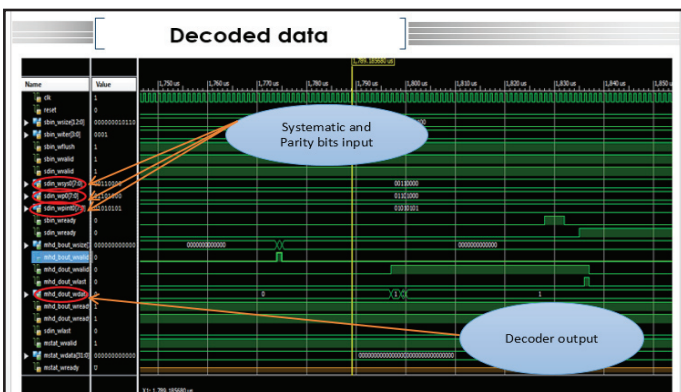


Fig. 9: The Testing Results of the DE-Code Block.

3. Turbo Encoder and Decoder verification

The verification is designed and implemented using a loopback test, where the Turbo Encoder output is applied to the Turbo Decoder input. The result of the verification test is pass when the decoder output is the same as the encoder input; which is clearly shown in Fig. 10.

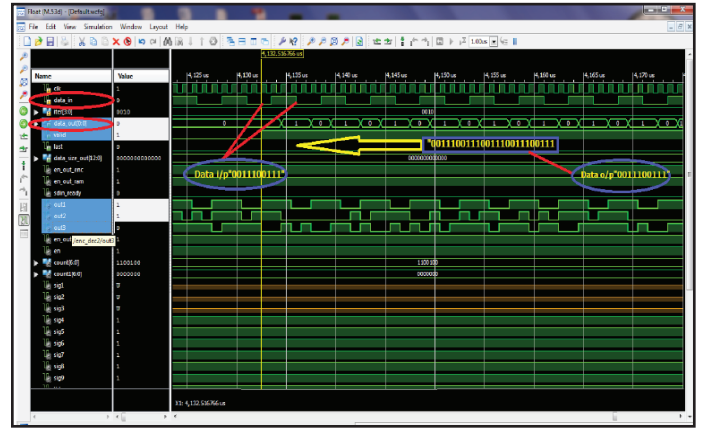


Fig. 10: The Encoder and DE-Code Verification

D. Rate Matching and De-Rate Matching

The following subsections introduce the VHDL implementation of the Rate matching and De-rate matching blocks.

1. Rate Matching

The three parallel outputs of the Turbo Encoder block are applied to the Rate Matching input. The function of the Rate Matching block is to enhance the data security and make it having a high immunity against channel errors. The Rate Matching block consists of three sub-block interleaver, bit collection, and selection blocks as shown in Fig. 11.

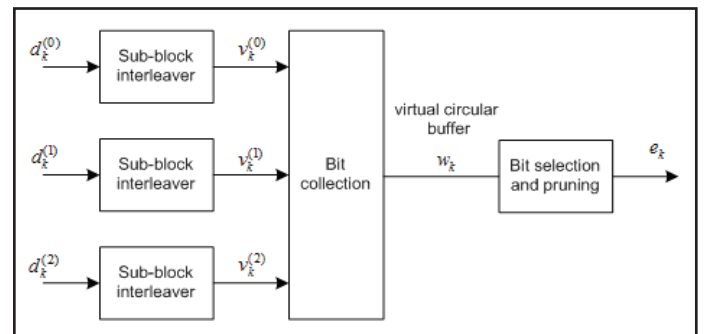


Fig. 11: Rate Matching Block for Turbo Coded Transport Channels [22].

The Sub-block interleaver operation is to reorder the input bit stream positions according to Release 10 standards that shown in Table 1.

Table 1: Inter-Column Permutation Pattern for Sub-Block Interleaver [22].

Number of columns $C_{subblock}^{TC}$	Inter-column permutation pattern $< P(0), P(1), \dots, P(C_{subblock}^{TC} - 1) >$
32	$< 0, 16, 8, 24, 4, 20, 12, 28, 2, 18, 10, 26, 6, 22, 14, 30, 1, 17, 9, 25, 5, 21, 13, 29, 3, 19, 11, 27, 7, 23, 15, 31 >$

The function of the bit collection and bit selection blocks are to convert the three parallel output from the sub-block interleaves into a one output sequence by grouping them according to the specification that is shown in fig. 12. It is shown that at each round one bit is taken from each sequence. A bit from $v_k(0)$ sequence

followed by a bit from $v_k(1)$ sequence then a bit from $v_k(2)$ sequence and so on. Fig. 13 shows the final testing results of the Rate Matching block.

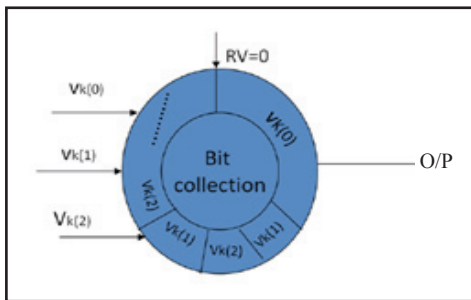


Fig. 12: The Transmission Bit Collection and Selection Operation

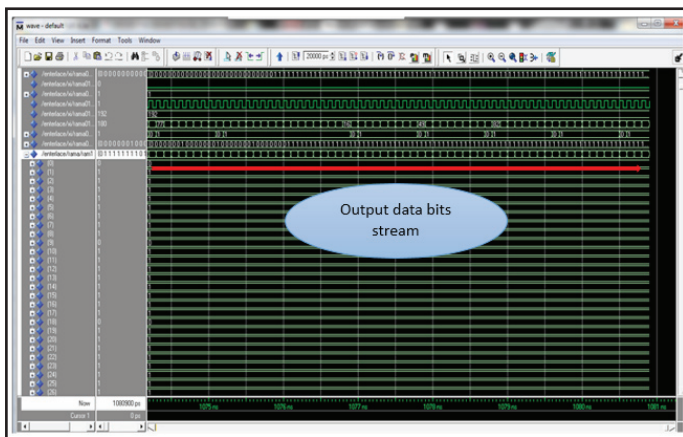


Fig. 13: The testing Results of the Stream Combining in Rate Matching Operation

2. DE-Rate Matching

The processes of the DE-rate matching block are the reverse of the operations of the Rate Matching block. Fig. 14 shows the testing results of the DE-rate matching. It is clear that the input is a one data sequence and the output is the three original data sequences.

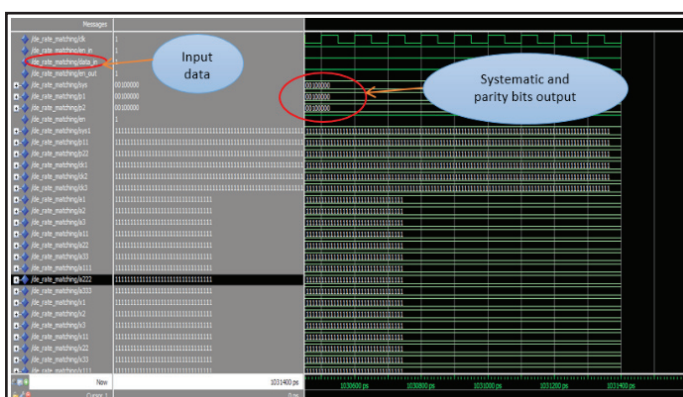


Fig. 14: DE-Rate Matching Testing Results

E. The Scrambler and De- Scrambler

In the following subsections, we will introduce the Scrambler and DE-Scrambler implementation process.

1. The Scrambler

The function of the Scrambler block is to increase the system security and prevent the long sequences of zeros or ones in the transmitted data to make the clock regeneration in the receiver easier. The Scrambler block is designed using the Pseudo Random

Sequence Generator (PRSG) with a length of 31 bit Gold sequence; which is shown in fig. 15.

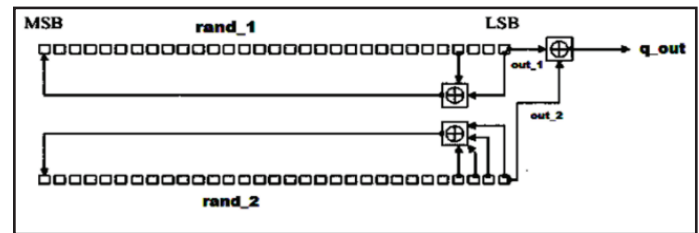


Fig. 15: The Pseudo Random Sequence Generator (PRSG).

The output from the Rate matching block is applied to the Scrambler input. The initialization of the rand_1 and rand_2 in the PRSG sequence are determined according to LTE-A Release 10 specification that is mentioned in section (7.2) in [21]. The PRSG sequence is implemented by using the VHDL code. The Scrambler output is the result of the X-oring operation between "q_out" sequence and the output of the Rate Matching block. Fig. 16 shows the simulation results of the Scrambler initialization process. It is shown that when the reset and enable values are ones, the Scrambler operates in the initialization process. When the reset is Zero and the enable is one, the Scrambler operate in the X-oring mode. Fig. 17 shows the testing results of the Scrambler block.

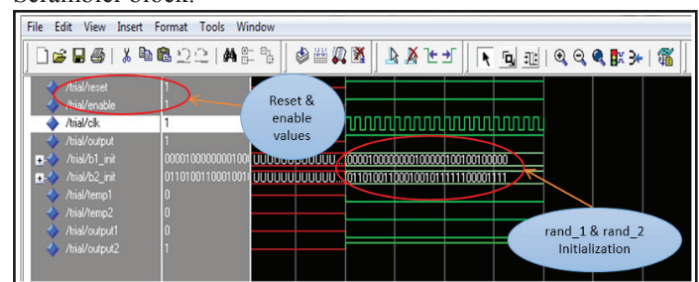


Fig. 16: The Scrambler Initialization

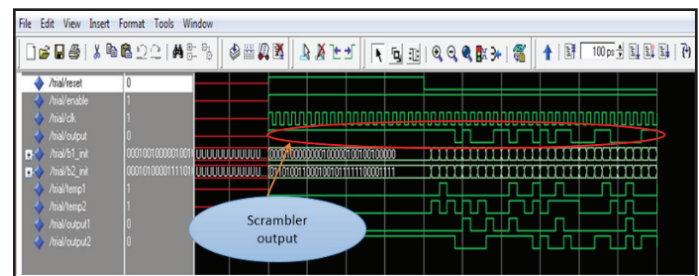


Fig. 17: The testing Results of the Scrambler Block

2. The DE-Scrambler

At the transmitter the operation of the DE-Scrambler is the reverse that of the Scrambler. Fig. 18 shows the testing results of the DE-Scrambler block.

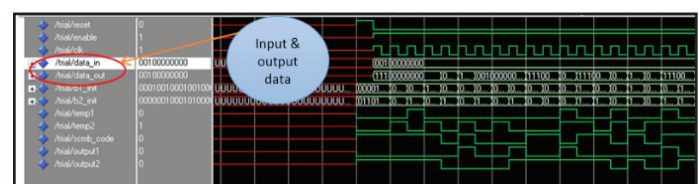


Fig. 18: The DE-Scrambler Results.

F. The Mapper and the DE-Mapper

The following sub-sections show the design and implementation of the Mapper and DE-Mapper blocks using the VHDL codes.

1. The mapper

The digital modulation constellation diagram represents the Mapper with type M-QAM with $M=16$. The Mapper input is the certain logic values that are the output data from the Scrambler block. This input is assigned by the baseband symbols; which are the I and Q components. Where I is the in-phase component and Q is the quadrature component. Fig. 19 shows the simulation results of the Mapper block.

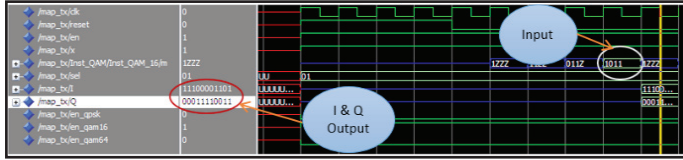


Fig. 19: Results of the 16-QAM mapper.

2. DE-mapper

The DE-Mapper block at the receiver has the reverse operation of the Mapper block at the transmitter. The DE-Mapper input is the complex QAM symbols that are received from the DE-Scrambler block. Fig. 20 shows the testing results of the De-mapper block where the complex QAM symbols are represented by the I and Q values and the output is four bits for every symbol.

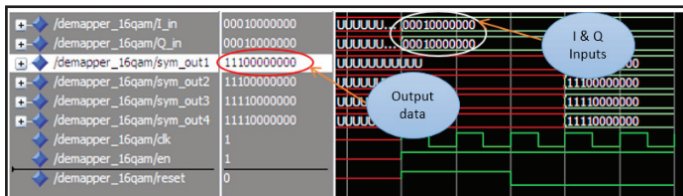


Fig. 20: The Testing Results of the De-mapper Sub Block.

G. The Layer mapping and DE-Layer mapping and The Precoding blocks

The Layer Mapping block function is to map the complex-valued modulation symbols that are the output from the Mapper block to one or several transmission layers (antenna ports). For 2x2 MIMO system, the Layer Mapping block distributes the complex-valued modulation symbols between two transmission layer with two code words according to release 10 specifications (table 6.3.3.2-1 in section 6.3.3.2) [21].

The function of the Pre-coding block is to multiply the complex-valued modulation symbols on each layer by a specific matrix for the data to be transmitted from the two antenna ports simultaneously. The linear combination of the two data streams at the two receiver antennas results in a set of two equations and two unknowns, which are resolvable into the two original data streams. The pre-coding matrix is applied according to release 10 specification (table 6.3.4.2.3-1 in section 6.3.4.2.3) [21]. Fig. 21 and Fig. 22 show the final results of the Pre-coding block form two layers.

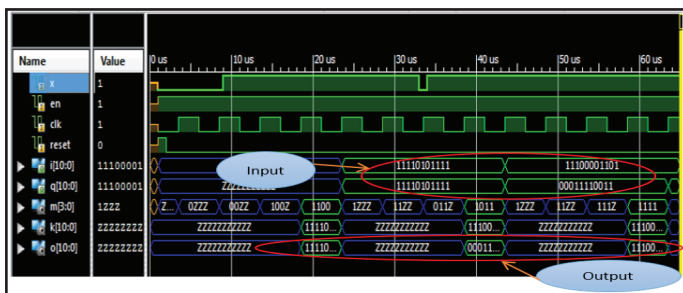


Fig. 21: The Precoding Final Results From Layer One

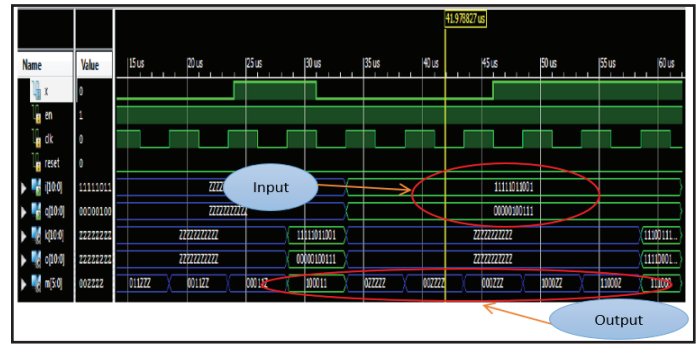


Fig. 22: The Precoding Final Results From Layer Two

H. The Resource Element Mapping and DE-Mapping

The Pre-coding symbols to be transmitted by the antenna ports are mapped to the resource elements block. The number of the available resource blocks is a function of the channel bandwidth as shown in Table 2.

Table 2: The Resources Block for Different Channel Bandwidth [23].

Channel bandwidth BW _{Channel} [MHz]	1.4	3	5	10	15	20
Transmission bandwidth configuration N _{RB}	6	15	25	50	75	100

For the chosen LTE-A configuration, at 3MHz bandwidth the system have 15 resource block (RB), each one contain 12 subcarriers, then the total effective subcarrier number is 180 subcarrier (the number of the system RB multiple by the number of subcarriers in each RB). According to the Downlink resource grid shown in Fig. (6.2.2-1) in the LTE-A specification [21], it is implemented by generating a RAM of length 256 words and width of 22 bits. According to the specifications, a total of 180 locations is used, and the remaining locations are filled by zeros. We use a RAM length of 256 for the next IFFT block. The size of the IFFT block must equal to 2^n , where n is an integer. So, the nearest size for the IFFT for the 180 sub-carrier is $2^8=256$. Then we have 76 (256-180) free sub-carriers so, the RAM was filled by 38 zeros at the beginning and at the end of the OFDM symbol. The data are located at the middle of the RAM. The test results of the implemented data are shown in Fig. 23a, b and c.

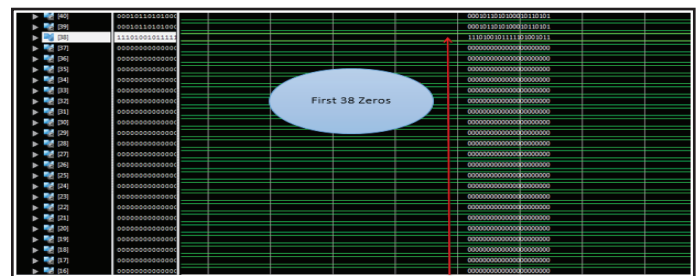


Fig. 23(a): The RAM 38 Zeros at the Beginning

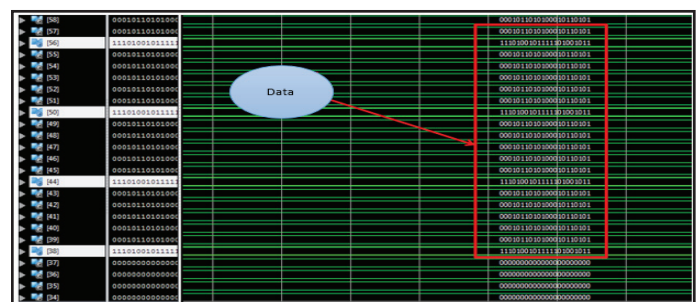


Fig. 23(b): The Data in the Middle of RAM.

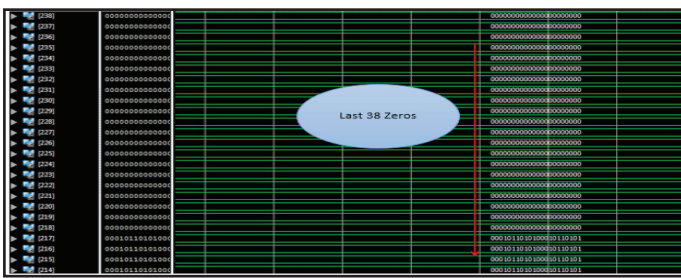


Fig. 23(c): The RAM 38 zeros at the end.

I. The OFDM Signal Generation

The next stage after The Resource element Mapping is the OFDM block. The OFDM block consists of an IFFT block and cyclic prefix insertion that is shown in Figure 24.

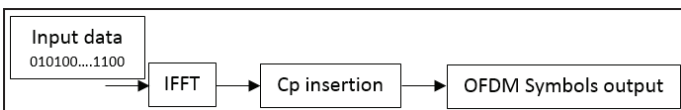


Fig. 24: The OFDM Block Diagram

The following sub-section introduces the implementation of the IFFT block, the Cyclic Prefix sub-block (OFDM), the cyclic prefix removal block and the FFT sub-block (DE-OFDM).

1. IFFT and Cyclic Prefix Sub Block

The last two operations of the transmitter are the IFFT and the Cyclic Prefix (CP) insertion. The function of the IFFT block is to increase the bandwidth spectral efficiency by using the orthogonal frequency division while the function of the CP insertion block is to prevent the transmitted data from the Inter-Symbol Interference (ISI) and the Inter-Carrier Interference (ICI). The IFFT block (with a size of 256) and the CP insertion was implemented using Xilinx core. According to Release 10 specification, the last 144 samples in the OFDM symbol (for short CP) we will be copied at the start of it. Fig. 25(a) and Fig. 25(b) show the implementation results of the IFFT Xilinx core. Fig. 26 shows the simulation results of the Cyclic Prefix process.

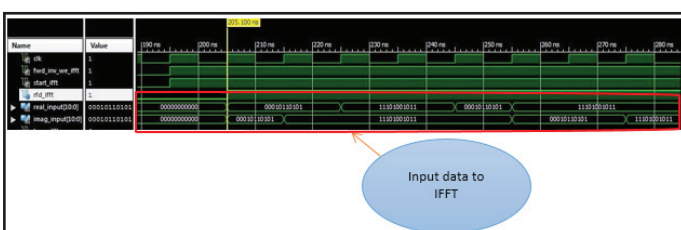


Fig. 25(a): The Input to the IFFT Block

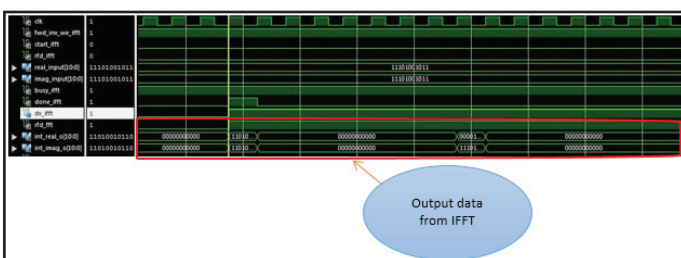


Fig. 25(b): The Output From the IFFT Block.

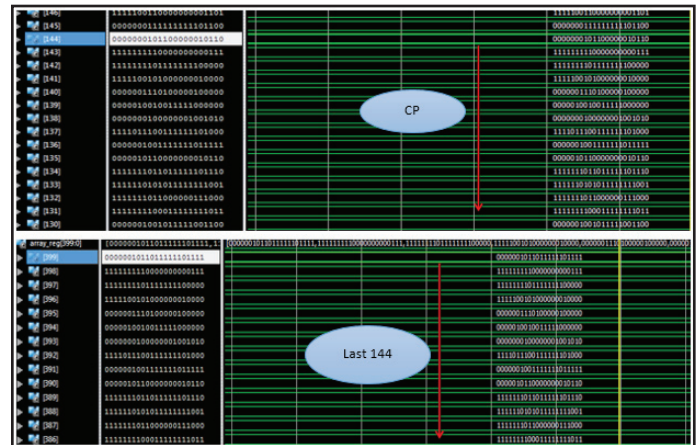


Fig. 26: The Cyclic Prefix process.

2. Cyclic Prefix Removal and FFTsub Block

At the receiver, the cyclic prefix removal and FFT blocks have the reverse operations of the OFDM block at the transmitter. The CP removal sub-block removes the first 144 samples of the received OFDM symbol. The FFT block is implemented using a Xilinx generating core. Fig. 27 shows the simulation results of the FFT Xilinx core.



Fig. 27: The output from FFT block.

J. Time and Frequency Synchronization Blocks

The first two blocks in the receiver are the Time and Frequency Synchronization blocks. The function of the Time Synchronization block is to determine the start of the OFDM symbol while the function of the Frequency Synchronization block is to detect the frequency offsets that occurs due to the channel effects (like the Doppler shift and the carrier frequency mismatching between the transmitter and receiver oscillators). To determine the Time and Frequency Synchronization values we will depend on the fact that the last 144 samples in the OFDM symbol are repeated in the start as shown in Fig. 28.

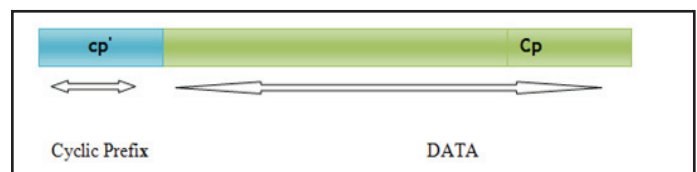


Fig. 28: OFDM Symbol

The Synchronization process is done by correlating the received symbols with its delayed version by the OFDM symbol time T then repeating this operation 144 times (CP length) to calculate the summation of the resultant values each time to get the correlation value at this point. Then we will shift one bit in the received symbol and repeated the previous correlation process. Then, the max correlation result is chosen and putted in the polar form. The amplitude and the phase at the max correlation value represent the OFDM start position and the frequency offset values respectively. Fig. 29 shows the correlation process to obtain the Time and Frequency Synchronization values. The received OFDM symbol is delayed by the OFDM symbol time T . The following equation is used to calculate the correlation output $X(t)$:

$$x(t) = \int_0^{Tg} r(t-\tau) r^*(t-\tau-T) dt$$

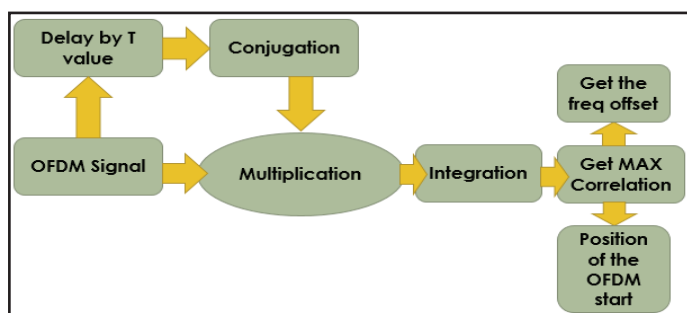


Fig. 29: Frequency and Timing Synchronization Through Cross Correlation

The Time and Frequency Synchronization processes are designed and implemented by using the VHDL codes. The following subsections are introducing the implementation of the Time and Frequency Synchronization blocks.

1. The Time Synchronization Block Simulation

The Register-Transfer Level (RTL) Schematic and the simulation results of the time synchronization block are shown in fig. 30 and fig. 31 respectively. It is clear that the start of the OFDM symbol was detected at sample number 144 as it should be.

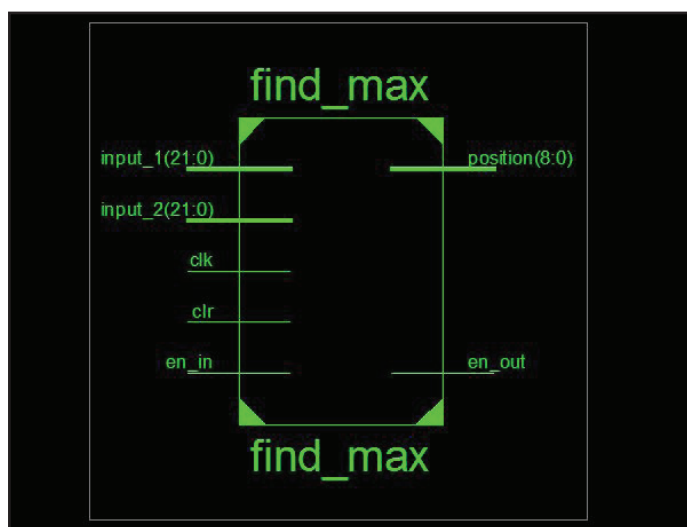


Fig. 30: The Time Synchronization RTL Schematic.

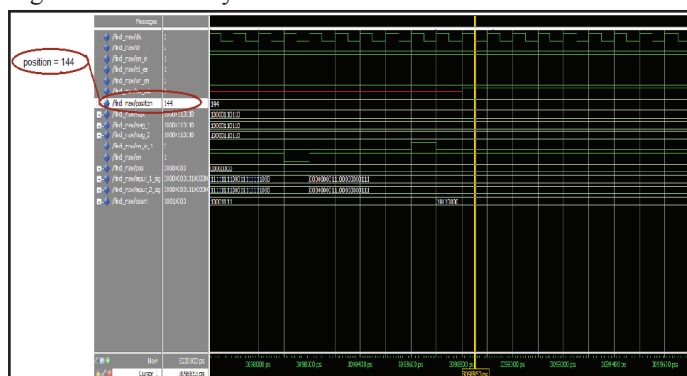


Fig. 31: The Time Synchronization Block Testing Results.

2. The Frequency Synchronization Block Simulation

The RTL Schematic and the testing results of the Frequency Synchronization block are shown in Fig. 32 and Fig. 33 respectively.

By notice, the simulation result figures the value of the frequency offset is zero because there no channel effects are applied.

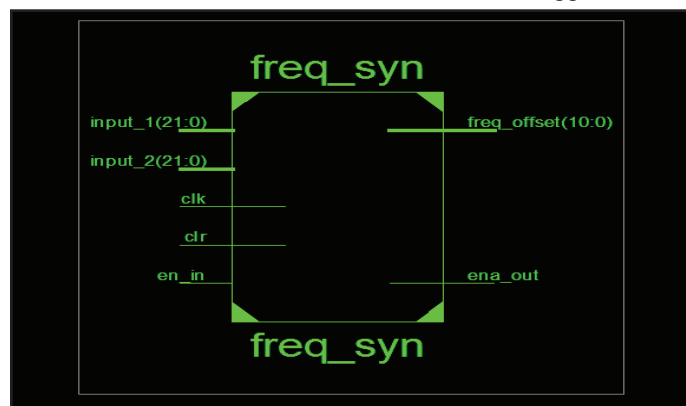


Fig. 32: The Frequency Synchronization RTL Schematic.

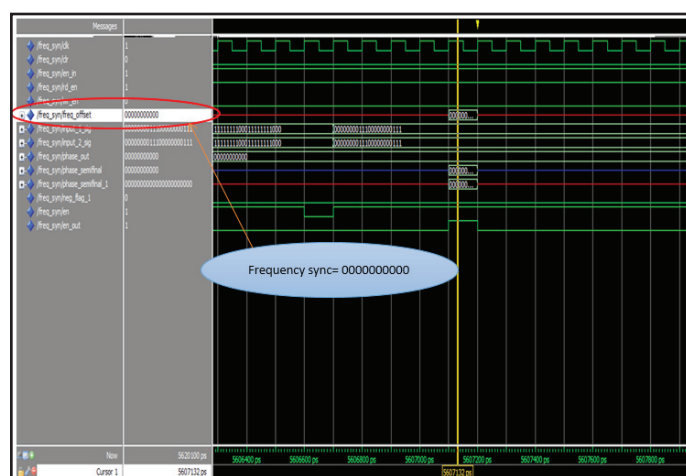


Fig. 33: The Frequency Synchronization Testing Results

III. The Full System Verivation

The overall system verification is done by comparing the transmitter input to the receiver output with no channel effects. The transmitter input was represented by two OFDM symbols of 192 bits length and have the pattern 0101010.....01010. Fig. 34 shows the Transmitter input while fig. 35 shows the Receiver output data. It is clear that the transmitter input coincides with the receiver output. Then the full system verification is done.

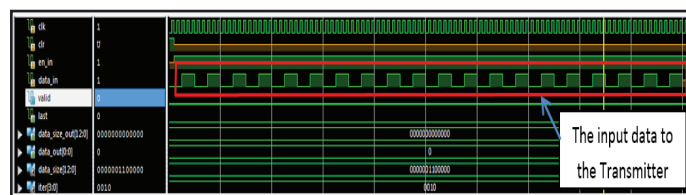


Fig. 34: The Transmitter Input

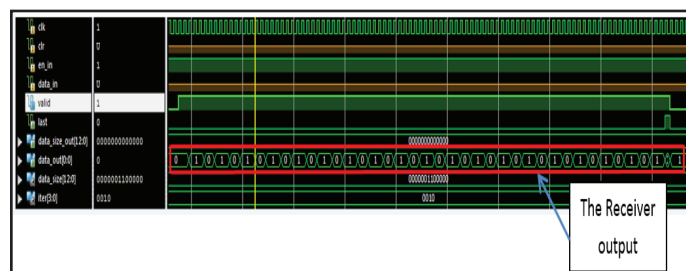


Fig. 35: The Receiver Output.

IV. The System Utilization

After implementing all the building blocks of the transceiver on FPGA Virtex 6, it is interesting to get out chip utilization for the whole system. In the following sub-section, the full system utilization will be introduced for the downlink LTE-A baseband single carrier and it is area optimization strategy.

A. The Full System Utilization

The single carrier baseband system (Transmitter and receiver) resources utilization table from Virtex 6 FPGA is shown in Table 3. It is clear that the LTE-A physical layer utilizes a small fraction of the resource blocks from Virtex 6. As shown in the table the number of used slice registers and the number of the look-up tables (LUTs) are very small, 1% and 4% respectively. The number of fully LUT-FF pairs (utilization efficiency) is high (62 %); which means a good utilization of the FPGA resources comparing by the previous design in [24].

Table 3: The Full System Utilization on Virtex 6.

Device Utilization Summary (estimated values)				
Logic Utilization	Used	Available	Utilization	
Number of Slice Registers	3991	301440	1%	
Number of Slice LUTs	6383	150720	4%	
Number of fully used LUT-FF pairs	3976	6398	62%	
Number of bonded IOBs	85	600	14%	
Number of BUFG/BUFGCTRLs	2	32	6%	

B. The Area Optimization Utilization

From Xilinx ISE Design Suite 13.3 Design Goals and Strategies, the area optimization strategy was simulated. Table 4 shows the full system utilization by applying the area reduction design goal. By comparing the full system utilization table mentioned in the previous sub-section and the full system utilization table with area reduction strategy we notice that the numbers of slice registers is reduced from 3991 to 3968 and the slice LUTs are reduced from 6383 to 5567. Also there is an increase in the utilization efficiency (the number of fully LUT-FF pairs) from 62% to 71%.

Table 4: The full system utilization on Virtex 6 with the area reduction design goal.

Device Utilization Summary (estimated values)				
Logic Utilization	Used	Available	Utilization	
Number of Slice Registers	3968	301440	1%	
Number of Slice LUTs	5567	150720	3%	
Number of fully used LUT-FF pairs	3968	5567	71%	
Number of bonded IOBs	85	600	14%	
Number of BUFG/BUFGCTRLs	2	32	6%	

V. The Carrier Aggregation scenario

To increase the data rates and system capacity the Intra-band contiguous carrier aggregation scenario was applied. Two Component Carriers (CCs) are aggregated to double the system data rate. Fig. 36 shows the definition of aggregated channel bandwidth, aggregated channel bandwidth edges and the channel bandwidth for the contiguously aggregated component carriers.

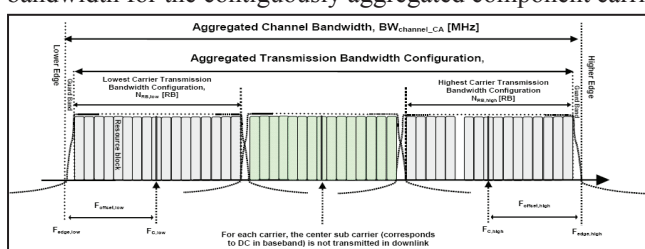


Fig. 36: Contiguously Aggregated Component Carriers [23].

The Downlink LTE-A simulation is designed to support 6 MHz CA with two CCs each one has a 3 MHz as a bandwidth. The center of the aggregated carriers shifted to baseband (0 Hz) and the center of two Component Carriers is -1.5 and 1.5 MHz respectively. The simulation of CA scenario is done by using Matlab codes, to plot the CA power spectrum, because the VHDL simulator gives the frequency components values but the simulator is unable to plot the components spectrum. The CA calculation parameters are determined according to 3GPP release 10 sections (5.6 and 5.7) [23]. Fig. 37 shows the Power Spectrum simulation using the Matlab program for the CCs. The CA Matlab simulation parameters are shown in fig. 38.

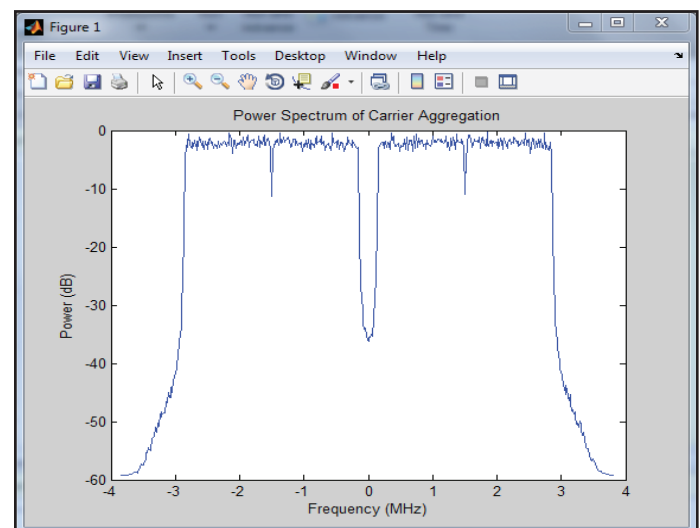


Fig. 37: The Power Spectrum of the Component Carriers

- F_c_low: -1.500 MHz
- F_edge_low: -3.000 MHz
- F_c_high: 1.500 MHz
- F_edge_high: 3.000 MHz
- BW_channel_CA: 6.000 MHz
- F_offset_low: 1.500 MHz
- spacing: 3.000 MHz
- F_offset_high: 1.500 MHz

- Component Carrier 1:
Lower band edge: -2.850 MHz
Upper band edge: -0.150 MHz
- Component Carrier 2:
Lower band edge: 0.150 MHz
Upper band edge: 2.850 MHz

Fig. 38: The Matlab Simulation Parameters for the Two CCs.

VI. Conclusion

In this paper, a complete LTE-advanced downlink physical layer transceiver with 2x2 MIMO technique and the Intra-band contiguous CA type has been designed and implemented according to the 3GPP Release 10 specification. All the stages of the LTE-Advanced Release 10 downlink physical layer, including the transmitter and the receiver, are modeled using Xilinx® ISE® Design Suite version 13.3 and implemented on Virtex 6 XC6VLX240T FPGA kit. The implemented building blocks include the time and frequency synchronization function in the receiver. It was found that the whole LTE-Advanced downlink physical layer consumes a small fraction of all the logic blocks. Moreover, the application of the CA scenario and the 2x2 MIMO

technique increase the system data rate and its throughput twice. On the other side the CA scenario needs bandwidth extension. So the CA advantage is tradeoff with the bandwidth.

VII. Future work

In the future it is planned to implement the complete LTE-Advanced physical layer including the uplink. Enhancements can be done with the LTE-advanced starting with Release 12 Specifications.

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