Design of IEEE 1149.1 Testing Bus Controller IP Core

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Abstract
This paper introduces the design and implementation of a testing module based on the fundamentals of the IEEE 1149.1 Boundary-Scan (BS) standard. The presented module illustrates the usage of the IEEE 1149.1 standard for in-circuit interconnect testing thereby increasing observability and controllability for single/ multiple devices. The module covers the standard architecture, protocol, and required instruction sets. It includes a TAP controller, scan register, other Boundary Scan registers necessary to execute the BS commands like: EXTEST, BYPASS and SAMPLE/ PRELOAD. Furthermore, it provides information and animated boundary-scan test simulations. The presented work is divided into two main parts; software creation and hardware implementation. The user-friendly software module presents the ability to perform the mandatory testing operations in the BS standard in order to validate the hardware reliability. The hardware implementation is a complete design of the BS architecture together with a circuit under test.

Keywords
Boundary-scan (BS), Field-Programmable Gate Array (FPGA), Integrated Circuit (IC), Automatic Test Equipment (ATE), Unit-Under-Test (UUT), ball grid arrays (BGA), Chip Scale Package (CSP), chip on board (COB), Test Access Port (TAP).

I. Introduction

For decades, In-Circuit Test based on Automatic Test Equipment (ATE) featuring access to the Unit-Under-Test (UUT) through Bed-Of-Nail adapter was the workhorse for manufacturing test engineers [a]. Nowadays, fine pitch components like ball grid arrays (BGAs) and Chip Scale Package (CSP) or components that completely dispense with the casing - such as chip on board (COB), are extensively used. These new package technologies and the connection density that comes with them cause trouble for bed-of-nail fixture based testers, [2-3]. If the raster of the connections gets narrower, then inevitably the probes of the bed-of-nails, too, have to be placed closer to each other. This increases fixture cost and ultimately physical limitations will inhibit higher density. The traditional In-Circuit tester cannot be used due to the lack of the accessibility of the nodes. Here the idea of Boundary Scan came in. Boundary Scan principle is replacing the external probes of a test fixture with device-internal ones, the so-called "Electronic nails", [3]. In boundary scan technique, the virtual probing increases the controllability and observability. Using an appropriate set of boundary scan test patterns, most of the interconnections on a circuit board can be checked for the continuity and short circuits [4]. The IEEE 1149.1 BS standard [5] provides a foundation other standards have been building upon. Ongoing standardization efforts continue to exploit and improve other standards based on the IEEE 1149.1 BS standard [6-8]. These standards support a TAP-based access to internal chip test features in a standardized manner, [9]. This section provides a general overview of the operation of a component compatible with this standard and provides a background to the detailed discussion in a later section. The standard defines a boundary scan interface that consists of a 4-pin Test Access Port (TAP) as defined in the standard, TAP controller, instruction register and decoder, BYPASS register and Boundary Scan register as shown in fig. 1.

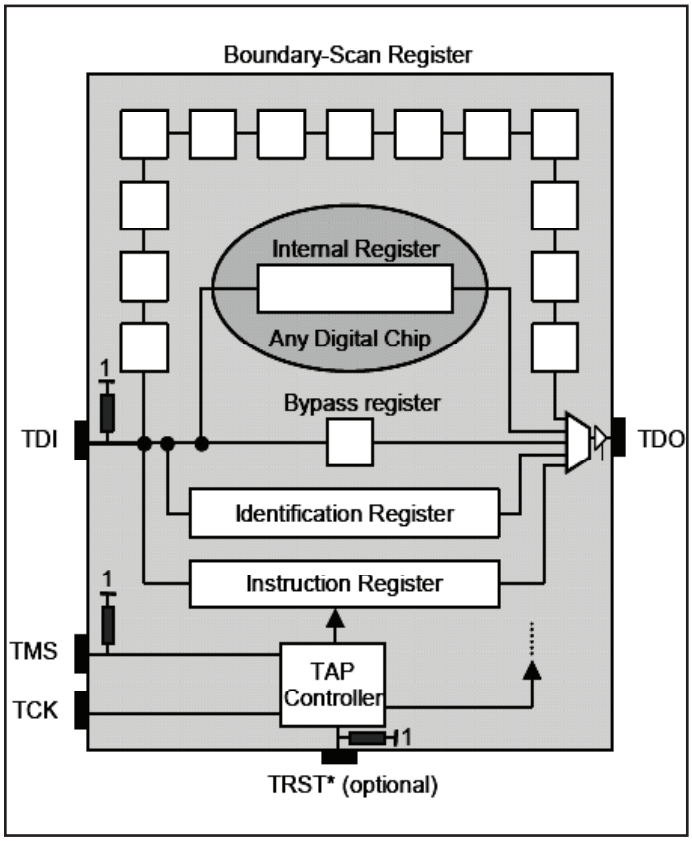


Fig. 1: Architecture of 1149.1

II. Boundary Scan Testing Module (BSTM)

Fig. 2 illustrates the block diagram of the proposed module with typical JTAG interface. The proposed testing architecture mainly a user-friendly GUI- driven software module that is responsible for executing all of the BS 1149.1 (mandatory/optional) commands. The software module has built in memory to generate the test vectors and to hold the designer's prescribed output to later, compare it with the measured output in order to validate the IC/PCB right performance, [12]. A PC/notebook is used to test the UUT via a parallel port interface. To emulate this testing architecture, a sample design with a Circuit under Test (CUT) is proposed, simulated and Downloaded on the Spartan Xilinx XC3S200 FPGA chip. The hardware implementation is tested using the interface through the PC parallel port that supplies all required signals. All required test circuitry is embedded in the integrated circuits and the control of the test circuitry is supplied from the TAP controller (TAPC). Finally, the TAPC is controlled via the parallel port of the PC. Thus, the PC is used as a master controller and the TAPC is used as a slave controller. The proposed idea of the software module solves the testing problem of digital VLSI circuits using traditional ATE.

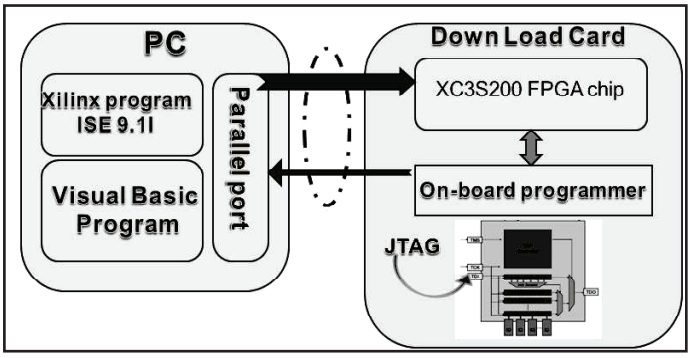


Fig. 2: Block Diagram of the Module With a Typical JTAG Interface

A PC is used as ATE controller to control the testing operation where its parallel port is used to apply the different digital test vectors to the unit under test (UUT). On the other hand, the serial test data output is read through the parallel port and compared with the pre-stored data on the PC in order to check its validity. Controlling the data lines of the parallel port is accomplished by using visual basic program that will be executed as a test program.

III. Software Module

In the proposed software module, the various operations (mandatory/optional) of the 1149.1 BS standards are button-driven. Each button recalls an independent procedure of instructions pertinent to the corresponding BS operation. A Microsoft windows is selected to be the operating platform for the proposed module Microsoft Access Database with graphical interface is used to enter golden expected test data-output. In the proposed software module, simulation of chip operation can be done in two modes; the TAP Controller Mode and the Command Mode. The first provides a very detailed illustration of operation of BS registers and the TAP controller. Furthermore, it helps to understand all the needed basics of the BS 1149.1 standard. It Focus on the methods to standardize access to these features for chip, board, and system testing and debugging. The Command Mode can be used for faster simulation of BS commands like EXTEST, SAMPLE/PRELOAD, BYPASS, etc. with different predefined input data.

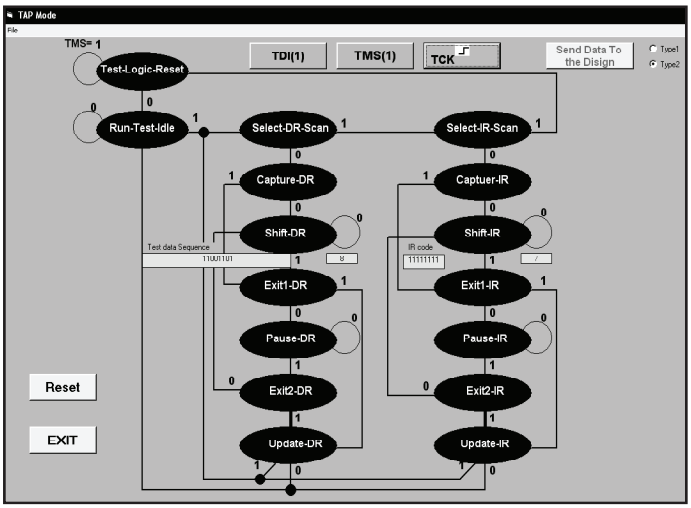


Fig. 3: TAP Controller

The control signals (TMS, TCK, and TDI) are combined and recorded all the transitions as a digital test vector input to the design in decimal format. The output results of TDO are extracted from the timing simulation and stored in a file as expected results to compare it with measured output from the chip. The TAP Controller simulation mode is illustrated in Fig. 3. In this mode, when shifting in needed instructions and test data, one should be careful. Since, the Test Access Port consists of only TDI, TDO, TMS (Test Mode Select) and TCK (Test Clock) I/O pins. All the instructions and test data can be shifted in via the TDI input only. The TAP Controller state together with an active instruction in the IR defines the operation and configuration of BS structures. For example, in order to select the EXTEST instruction, first, should reach the "Shift-IR" state of the TAP Controller by starting from the "Test-Logic-Reset" and moving through the following states: "Run-Test/Idle", "Select-DR-Scan", "Select-IR-Scan", etc. These state transitions are made by changing the TMS value and applying the TCK. The second phase is to make a shift in a proper bit sequence, which corresponds to the EXTEST instruction. For example, it is "00000000". After that, when the chip is in the EXTEST state, the test data should be inserted into the Boundary Scan Register. This is done in the same manner, but in the "Shift-DR" state.

For a certain test vector there is an expected output response, when the response is different from what was expected, the fault has been detected. The design implementation was tested using Model-Sim simulator and downloaded to the FPGA chip.

IV. Hardware Module

This subsection presents the design/implementation of the IEEE 1149.1 Boundary Scan hardware architecture on an FPGA chip as a real time application system. In addition, a simple CUT, comprised of four inputs and four outputs, is included. All design steps are processed for the implementation on the Spartan Xilinx chip XC3S200. The software module described in the previous subsection generates the test digital vector with the expected binary values of TDO produced from the model-Sim simulation. Both vectors are stored in table form. The test digital vectors are applied to the FPGA chip through the parallel port. The response, at every transition clock is read from the JTAG (TDO) and compared with the prestored expected value.

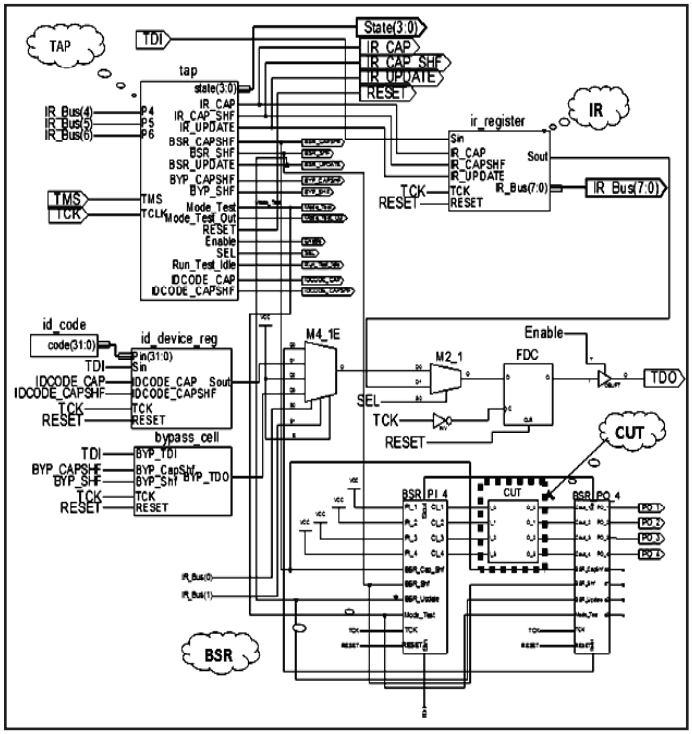


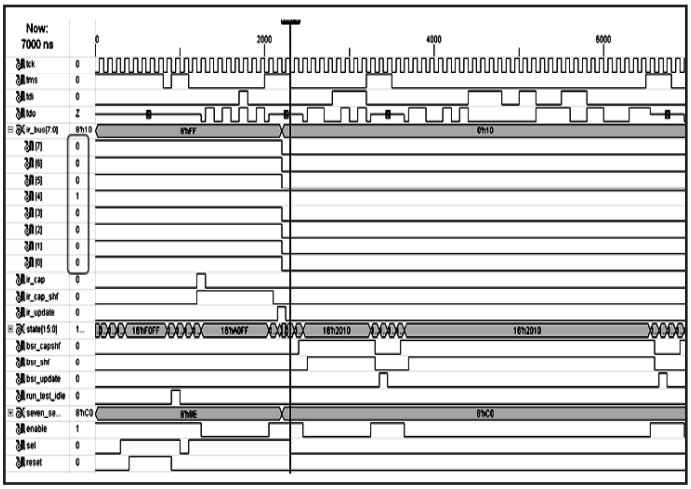
Fig. 4: Top-level Design of the Implemented Boundary Scan Architecture (CUT Included).

V. Experimental Results

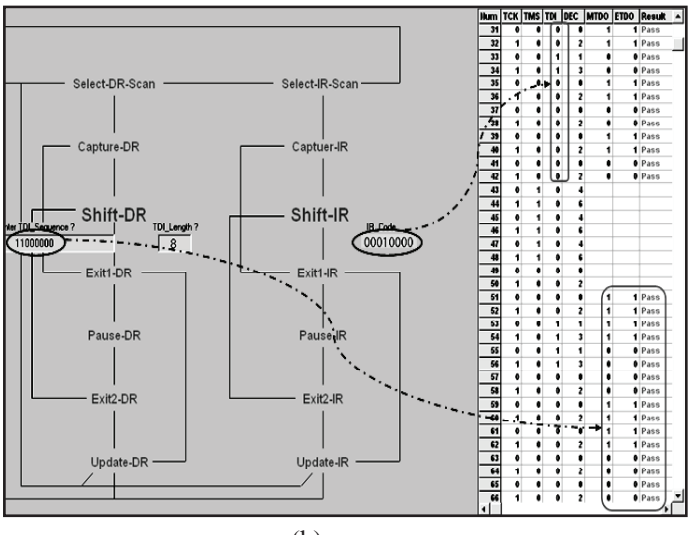
For evaluation of the proposed software module, different experiments are carried out on the complete system presented in the previous section. These experiments and the obtained results, as well as necessary validation comparisons, are introduced in the following subsections.

A. Sample/Preload Operation

In command mode, the input/output values are typed in the TDI text. The "Sample/Preload" command is then clicked, followed by clicking the "Send Data to the Design" command. Fig. 5 (a) shows the timing diagram representing the simulation for Sample/ Preload operation for the BS architecture with simple CUT, while Fig. 5 (b) illustrates the data Obtained after executing the above mentioned commands, and the generated values sent through the parallel port to the designed hardware on the Spartan Xilinx chip XC3S200. The "PASS" result verifies the implemented design.



(a)



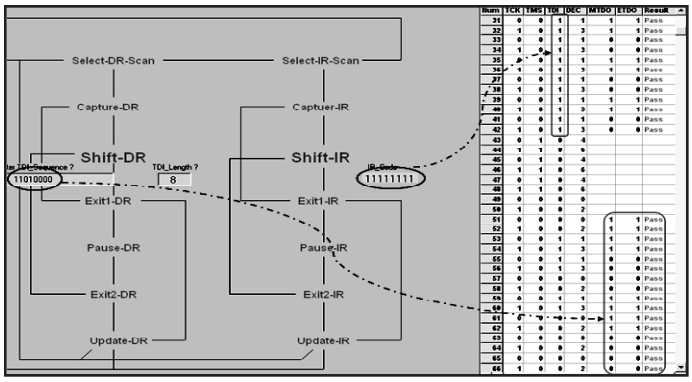
(b)

Fig. 5: Simulation for Sample/Preload Operation

B. BYPASS Operation

Fig. 6 (a) shows the timing diagram representing the simulation for BYPASS operation for the BS architecture with simple CUT, while Fig. 6 (b) illustrates the data obtained after executing the above mentioned commands, and the generated values sent through the parallel port to the designed hardware on the Spartan Xilinx chip XC3S200. The "PASS" result verifies the implemented design.

(a)

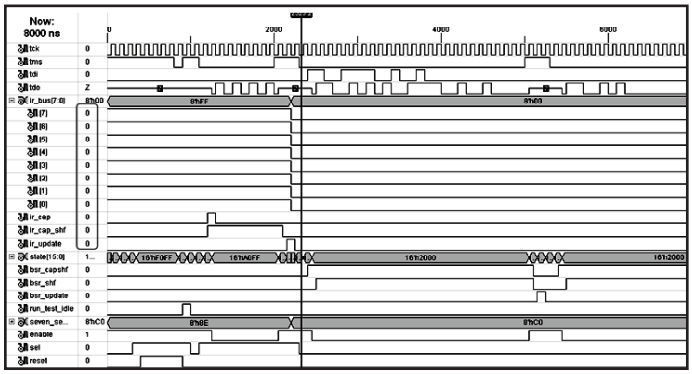


(b)

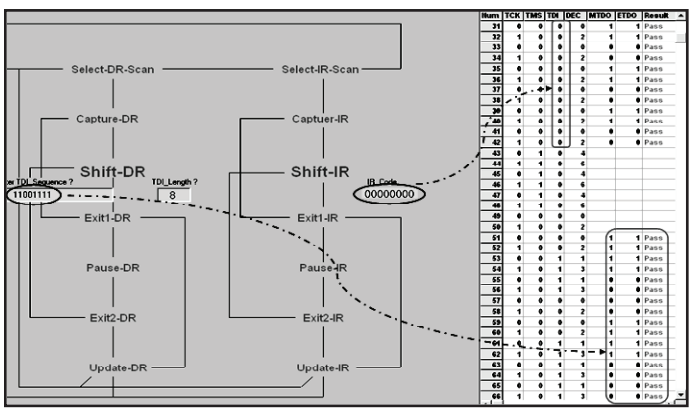
Fig. 6: Simulation for BYPASS Operation

C. EXTEST Operation

Fig. 7 (a) shows the timing diagram representing the simulation for EXTEST operation for the BS architecture with the simple CUT, while Fig. 7 (b) illustrates the data obtained after executing the above mentioned commands, and the generated values sent through the parallel port to the designed hardware on the Spartan Xilinx chip XC3S200. The "PASS" result verifies the implemented design.



(a)



(b)

Fig. 7: Simulation for EXTEST Operation

VI. Conclusion

This paper presents a proposed software module "BSTM", based on the IEEE 1149.1 Boundary scan standard, which can be used for testing and diagnosis of VLSI digital chips. Furthermore, the module can be used for training purposes to understand the basics/concepts of this specific standard. The proposed windows-based software module exceeds the capabilities of its published counterparts; thus, it is a very attractive substitution for portable ATE equipment. This approach is considered to reduce the cost of the traditional ATE. All designed simulated and downloaded on the Spartan Xilinx X3C200 chip.

VII. Acknowledgement

I express my deep sense of gratitude to my external guide Mr. Sreenivasa Rao, Somarouthu technologies, Hyderabad, for his invaluable guidance and encouragement in carrying out this project. I would like to take this opportunity to express my profound sense of gratitude to my guide Katta Vani, Assistant Professor, Nalla Malla Reddy Engineering College, for her constant guidance, supervision, motivation and encouragement all the way during the project, her annotations and criticisms are the key behind successful completion of this project work. Finally, I thank all the people who have directly or indirectly helped me through the course of this project.

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