Implementation of Baugh Woolley Multiplier by Using Novel Design RTP Reversible Logic Gate

[1]M.Ravindrababu, [2]K.Satyanarayanaraju
[1,2]Dept. of ECE, MVGR College of Engineering, Chintalavalasa, Vizianagaram, AP, India

Abstract
High speed and low power consumption are key requirements in any VLSI design. Conventional digital circuits dissipateenergy ***(KT ln2 joules/kelvin)*** as a bit of information is lost during the operation. Due to its low power dissipation, reversible logic circuit is more effective than conventional digital circuit. Reversible logic plays an important role in any low power circuit design. This paper presents a work on implementation of Baugh Woolley multiplier based on reversible logic gate technology. The structure of reversible gate Baugh Woolley multiplier consists of a Toffoli gate and an RTP reversible logicgate. The power dissipation of RTP gate full adder is less when compared to conventional full adder. The Baugh Woolley reversible multiplier is implemented in CMOS 0.13µm 1P2M technology has good performance in power dissipation when compared with other researches.

Keywords
Reversible Logic, Reversible Logic Gates, Low Power VLSI, Low Power CMOS Design.

I. Introduction

InVLSI design high speed and low power are two major concerns. Conventional digital circuits or irreversible gates like AND,OR,NAND,NOR,EX-OR, EX-NOR dissipates energy as a bit of information is lost during the operation. According to R landauer [2] irreversible gates have high power dissipation and hardware complexity. Information loss per bit in irreversible gate can be given as KT ln 2 joules/kelvin where K is Boltzmann constant and T is absolute temperature. At room temperature [2], the energy dissipation in conventional circuits is small and negligible but complex circuits can't be neglected. A logic which doesn't have any information losses are called the reversible logic. Reversible logic gates are used in number of research fields such as bioinformatics [4], low power CMOS design, optical, quantum computing, DNA computing thermodynamic technology, and Nanotechnology etc.

Multiplication is one of the fundamental blocks in almost all the arithmetic logic units.Multiplication can be considered as a series of repeated additions. The number to be added is called the multiplicand, the no of times it is added is called the multiplier and the result obtained is called the product. The basic operations involved in multiplication include generating and adding the partial products by using reversible logic.

II. Basic Reversible Logic Gates

The basic reversible logic gates are NOT gate, TOFFOLI gate, CNOT gate, FEYNMAN gate etc. All reversible gates have the following properties

1. The gate is said to be reversible, if there is one to one correspondence between its input and output. i.e.,the number of inputs equal to number of outputs.
2. The reversible gate doesn't allow fan-out condition.
3. There is no feedback in reversible logic gates.
4. The reversible gate uses minimum number of garbage outputs.
5. The designing of reversible circuit uses minimum number of circuit levels and gates.

A. Feynman Gate

The Feynman gate is a reversible logic gate shown in fig. 1. The input is I(A,B) and the output is O(P,Q). The truth table of Feynman gate is shown in Table 1.

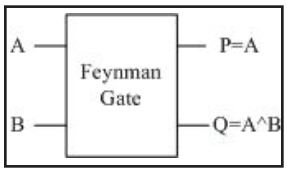

Fig. 1: Feynman Gate

Table 1: Feynman Gate

A	B	P=A	Q=A^B
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

B. NOT Gate

The NOT gate is one of the basic reversible logic gate shown in fig. 2. It is a 1x1 reversible logic gate. The truth table of NOT gate is shown in Table 2.

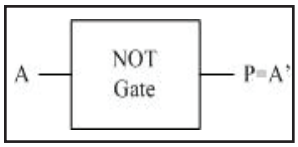

Fig. 2: NOT Gate

Table 2: NOT Gate

A	P= A'
0	1
1	0

C. TOFFOLI Gate

The TOFFOLI gate is a 3x3 reversible logic gate shown in fig. 3. The input is I(A B C) and the output is O(P Q R). The truth table of TOFFOLI gate is shown in Table 3.

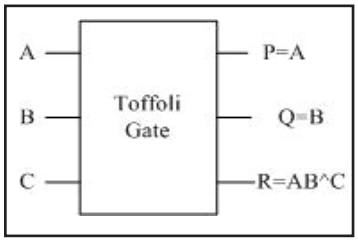

Fig. 3: TOFFOLI Gate

Table 3: TOFFOLI Gate

A	B	C	P=A	Q=B	R=AB^C
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

III. Baugh Woolley multiplier

The Baugh Woolley multiplier is an unsigned and parallel array multiplier. The architecture of Baugh Woolley multiplier is shown fig. 4.

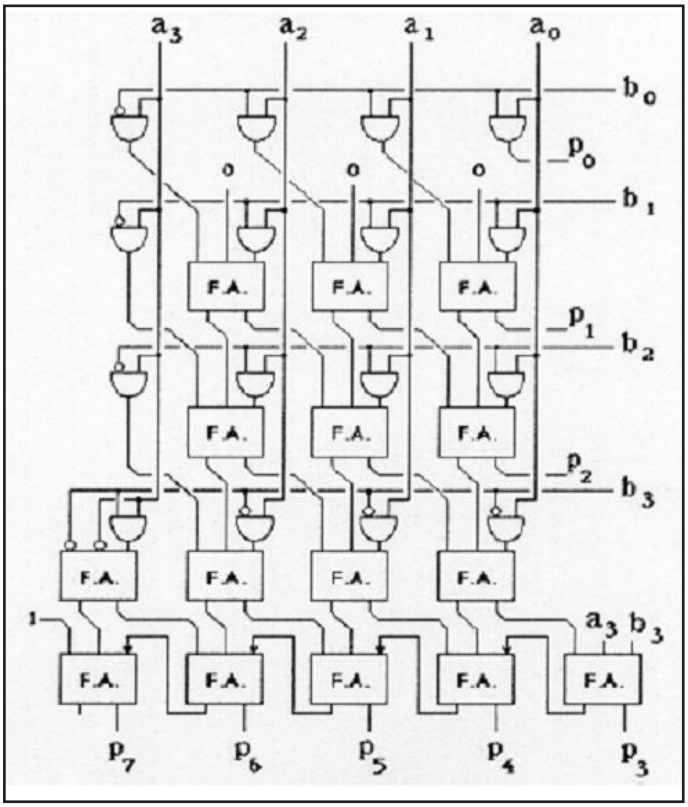

Fig. 4: Baugh Woolley Multiplier

The 4x4 parallel multiplier uses an AND for product term calculation and ultralow power full adder for multiple operand addition. Inverters are connected at the input of the AND gate to obtain complemented binary inputs.

A. Ultra-Low Power Full Adder (ULPFA) [1]

The ULPFA is based on low power XORgate and ultra-low power diode [1]. The ultralow power diode strongly reduces the leakage current when compared to a standard MOSFET diode. Implementation of ultra-low power full adder schematic diagram is shown in fig. 5.

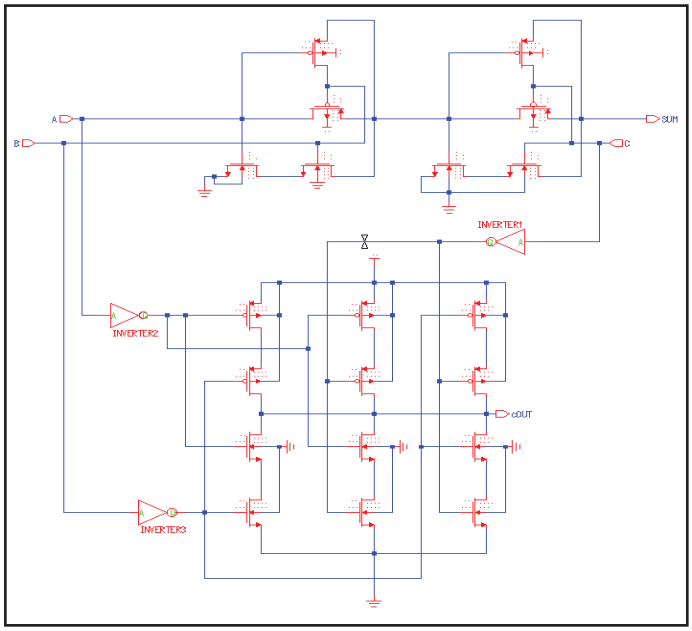

Fig. 5: Ultra Low Power Full Adder

1-bit ultralow power full adder and the AND gates are implemented in CMOS technology used in thedesign of 4x4 Baugh Woolley multiplier as shown in fig. 6.

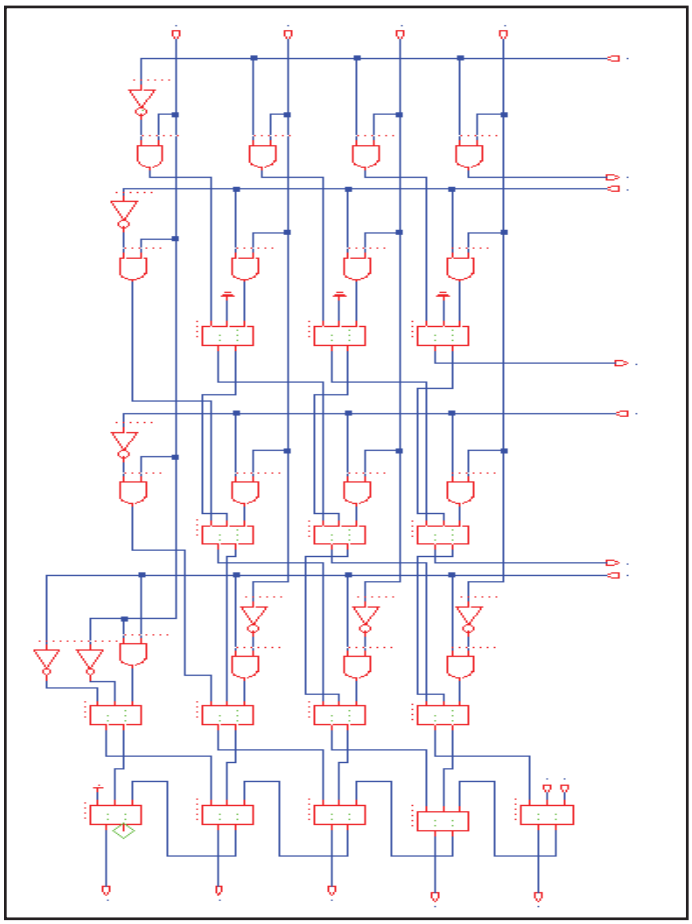

Fig. 6: Schematic Diagram of Baugh Woolley Multiplier Using Irreversible Logic Gates

IV. Proposed Reversible Logic Gate

A. RTP Reversible Logic Gate

I(A B C D) is input vector and O(P Q R S) is the output vector of RTP gate. The block diagram of RTP gate is shown in figure7.

The truth table of RTP gate is shown in table4. RTP gate is 4*4 reversible logic gatewhich can be mainly function as full adder which is faster and have less power dissipation when compared to ULPfull adder. The input and outputs of RTP gate given as I=(A,B,C,D) and O=(P=A,Q=AˆD,R=AˆBˆD,S=(AˆB)DˆABˆC). The input and output vectors for RTP gate to function as a full adder are I=(A,B,0,D) and O=(P=A,Q=AˆD,R=SUM,S=Cout)

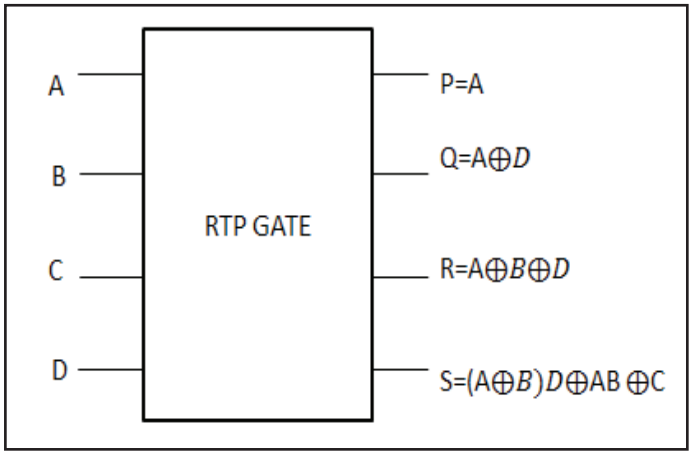

Fig. 7: RTP Reversible Logic Gate

Table 4: RTP Gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	0
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	1	0

The proposed RTP gate is implemented by using minimum number of transistors and reduces the power dissipation. The power dissipation of different types of 1- bit full adders are shown in Table 5.

Table 5: 1-bit Full Adder Comparison With =1V

Design	Power dissipation(nw)	Technology(µm)
Hybrid full adder	11.45	0.13
ULPFA	4.88	0.13
RTP FA	0.008	0.13

V. Proposed Design

For the implementation of unsigned BaughWoolley multiplier by using reversible logic gates, Toffoli gate for partial product generation and RTP gate for multi operand addition are used. The array multiplier requires 15 RTP full adders, 16 TOFFOLI gates and 8 NOT gates. The schematic design of multiplier is shown in fig. 8.

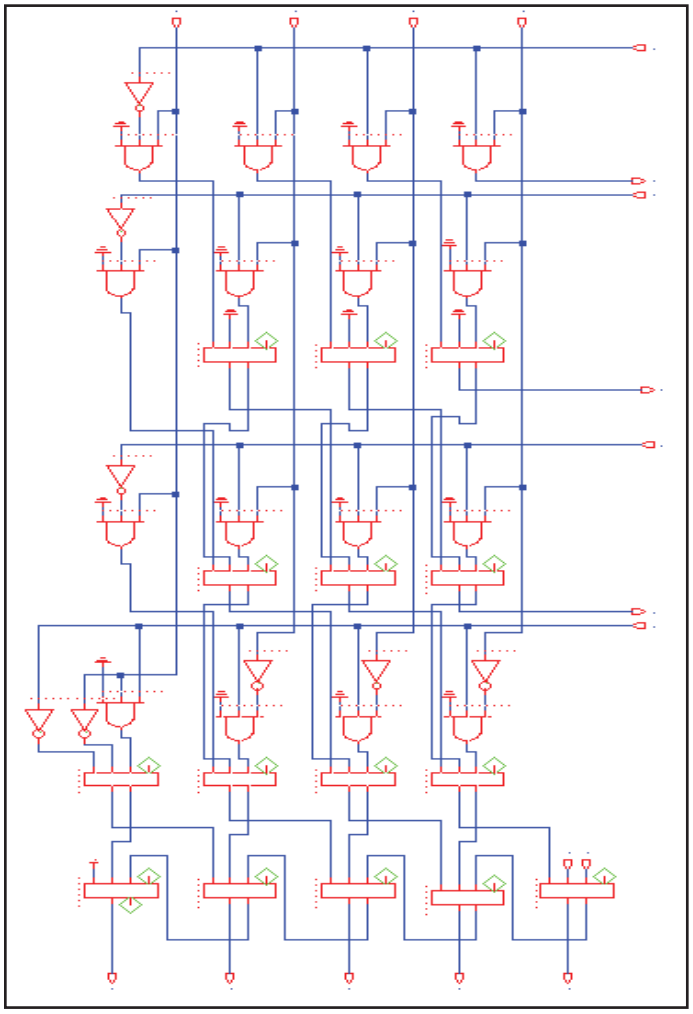

Fig. 8: Baugh Woolley Multiplier Using Reversible Gates

In the schematic design of Baugh Woolley reversible multiplier A0 to A3 and B0 to B3 are inputs and P0 to P7 are outputs. By using reversible logic gates the power dissipation is reduced according to R landauer [2]. The reversible Baugh Woolley multiplier is faster and has less power dissipation when compared to irreversible Baugh Woolley multiplier and other researches. The comparison is shown in Table 6.

Table 6: Comparison of Multipliers

Multiplier using gates	Power dissipation (µw)	Technology (µm)
Irreversible gates	64.49	0.13
Reversible gates	31.59	0.13

VI. Simulation and Post Layout

The Baugh Woolley reversible multiplier is simulated with ELDO simulator in mentor graphics tool. The simulated wave forms are shown in fig. 9.

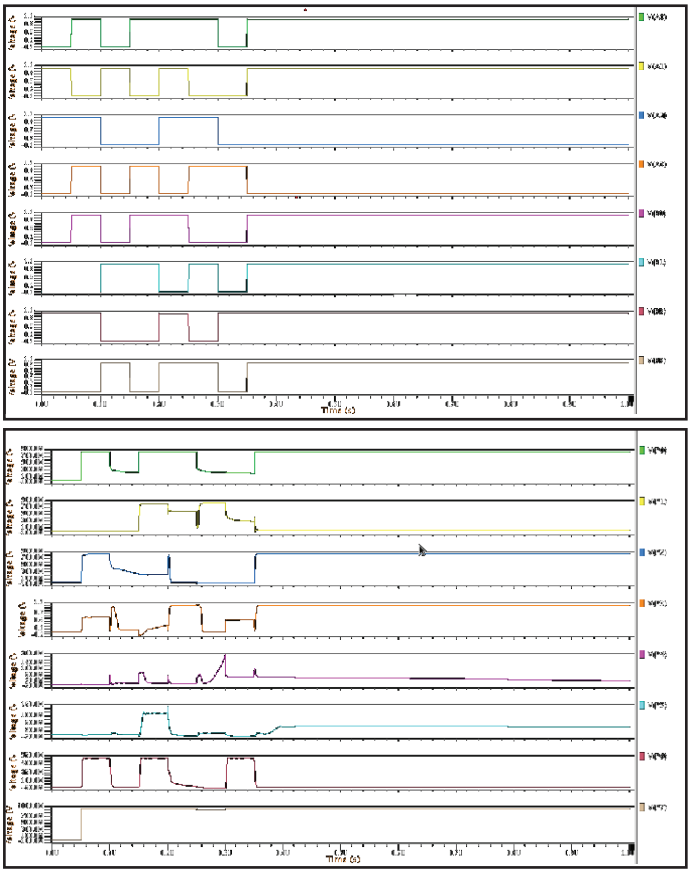

Fig. 9: Simulated Input and Output Wave Forms

The Baugh Woolley reversible multiplier, implemented in mentor graphics CMOS 0.13µm 1P2M technology, has good performance in power dissipation.The layout of Baugh Woolley reversible multiplier is shown in fig. 10.

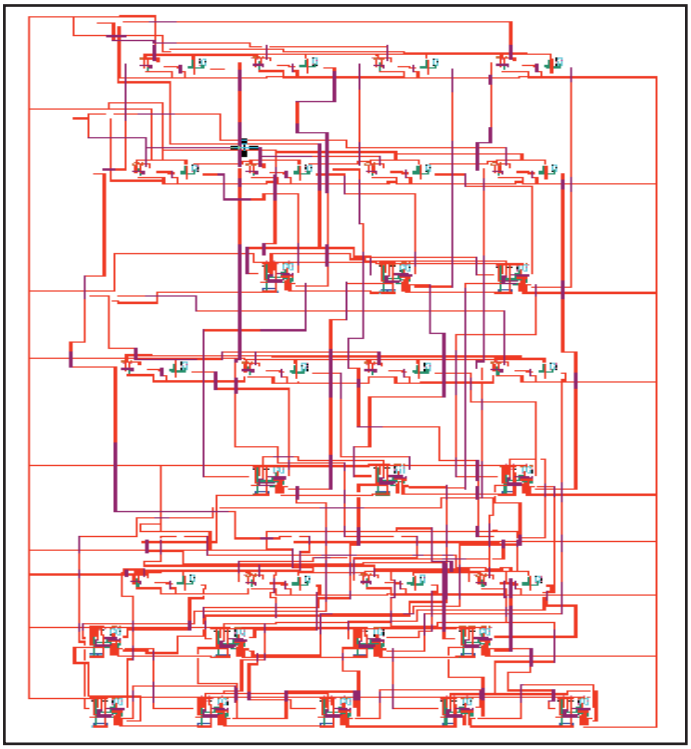

Fig. 10: 4*4 Baugh Woolley Reversible Multiplier Layout

VII. Conclusion

The proposed Baugh Woolley multiplier gives better results when compared to other Baugh Woolley multiplier techniques because the number of logic calculations gets reduced by using RTP reversible logic gate. The power dissipation of Reversible Baugh Woolley multiplier is low. The Proposed reversible multiplier is very useful in many applications in bioinformatics, low power CMOS design, optical, quantum computing, DNA computing and also thermodynamic technology, Nanotechnology.

References

[1] Ilham Hassoune, Denis Flandre, Ian O'Connor, Jean-Didier Legat,"ULPFA: A New Efficient Design of a Power-Aware Full Adder", IEEE transactions on circuits and systems—i: regular papers, Vol. 57, No. 8, August 2010.

[2] R. Landauer,"Irreversibility and heat generation in the computing process," IBM J. Res. Develop., Vol. 3, pp. 183–191, 1961.

[3] T. Sasao, K. Nimoshita,"Conservative logic elements and their universality," IEEE Trans. Comput., Vol. C-28, No. 9, pp. 682–685, Sep 1979.

[4] C. H. Bennet,"Logical reversibility of computation", IBM J. Res. Develop., Vol. 17, No. 6, pp. 525-532, 1973.

[5] M. Perkowski, A. Al-Rabadi, P. Kerntopf, A. Buller, M. Chrzanowska-Jeske, A. Mishchenko, M. Azad Khan, A. Coppola, S. Yanushkevich, V. Shmerko, L. Jozwiak,"A general decomposition for reversible logic", Proc. RM 2001, Starkville, (2001) pp. 119-138.

[6] Perkowski, M., P. Kerntopf,"Reversible Logic. Invited tutorial", Proc. EURO-MICRO, Sept. 2001, Warsaw, Poland, 2001.

[7] I. S. Abu-Khater, A. Bellaouar, M. I. Elmasry,"Circuit techniques for CMOS low-power high-performance multipliers," IEEE J. Solid-State Circuits, Vol. 31, No. 10, pp. 1535–1546, Oct. 1996.

[8] H. Lee, G.- E. Sobelman,"A newlow-voltage full adder circuit," In IEEE Proc. 7th Great Lakes Symp. VLSI, 1997, pp. 88–92.

Mr. M.Ravindrababu received B.Tech degree in ECE from Gudlavalleru engineering college. Pursuing M.Tech (VLSI) in MVGR college of Engg.

K. Satyanarayana Raju completed his B.TECH from MVGR College of engineering in 2004 and M.TECH degree from JNTUK in 2009 now he is working as assistant professor, Dept. of ECE, MVGRCE, Vijayanagaram. He has published 3 journal papers. Guided 4 M.TECH students. He is a member of IE. He is presently co-ordinator for IEEE student chapter. Research areas: 1. Digital Electronics and Communication Systems.