A Survey on Low Power CAM Circuits and Architectures

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Abstract
We survey recent advancements in theoutline of vast limit content addressable memory (CAM). A CAM is a memory that implements the search table function in a single clock cycle using committed evaluation circuitry. CAMs are particularly prominent in community routers for packet forwarding and packet classification; however they are additionally in a sort of other purposes that require fast table query. The fundamental CAM-design project is to decrease energy consumption related to the huge quantity of parallel active circuitry, without sacrificing speed or memory density. In this paper, we review CAM-plan procedures the circuit levels and at the architectural units. At the circuit level, we review low-energy matchline sensing schemes and at the architectural level we survey four approaches for reducing power consumption like bank selection scheme, static divided matched line architecture, Butterfly ML TCAM and MSML based CAM.

Keywords
Content-addressable Memory CAM, Bank Selection, Matchline Sensing, Review, MSML

I. Introduction

Lots of the memory devices store and retrieve data viaaddressing certain memory areas. This path turns intothe limiting factor for these systems that rely on fastmemory access. The time required to seek out the data savedin memory can be lowered if the data can be recognized by way ofits content alternatively than by way of its address. A memory used forthis intent is Content Addressable memories (CAM). CAM is used in applications the place search time is veryprimary and very brief. It's well suited for a couple ofservices like Ethernet tackle look up, data compression,and security or encryption data on a packet-by way ofpacket foundation for top efficiency data switches. It might probablyeven be operated as a data parallel or Instruction/Multiple Data (SIMD) processor. For the reason that CAM is an extension of RAM first, we have got to understand the RAM features to appreciate CAM. Mainly RAM has twooperations read and write i.e. the data saved in RAM canbe read or written however CAM has three operations read,write and compare [1]. The compare operation of CAMmakes it priceless in style of purposes like networkrouters. The networkrouter is that which forwards theincoming packets from the sender port to the appropriate actiondestination port by means of looking in to its routing table. Truly CAMs are used to design network routers forspeedy switch or forwarding of packets. We now take an extra unique look at CAM architecture.A small model is proven in fig.1. The fig. 1 suggests CAM consisting of four words, with each and every word containing threebits arranged horizontally (analogous to 3 CAMcells). There's a in match-line corresponding to each and every word (ML0, ML1, and many others.) feeding into match line sense amplifiers (MLSAs), and there's a differential search line pairsimilar to each little bit of the quest word (SL0, $SL0\overline{}$,SL1, $SL1\overline{}$, etc.). CAM search operation begins withloading the search-data word into the search-dataregisters followed by means of precharging all fit lines excessive,placing all of them quickly within the fit state. Next, thesearch line drivers broadcast the quest word onto thedifferential search strains, and each and every CAM core mobile phonecompares its stored bit towards the bit on itscorresponding search lines. Match lines on which all bitssuit stay within the precharged-excessive state. In shape linesthat have at least one bit that misses, discharge to ground. The MLSA then detects whether or not its suit line has amatching situation or miss. Ultimately, theencoder maps the healthy line of the matching vicinity toits encoded address [1].

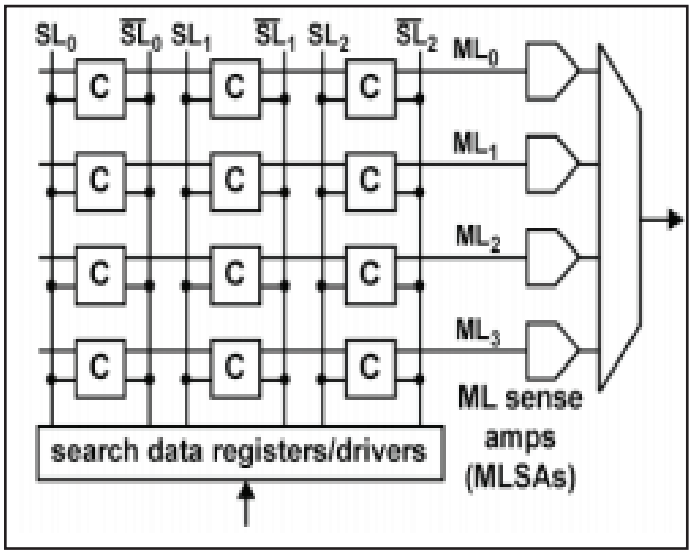

Fig. 1: Simple Schematic of a CAM

Content Addressable Memory (CAM) is a specialized type of memory used in very high speed search applications, mostly used as a Translation Lookaside Buffer (TLB). The TLB allows the translation of the virtual address of a CPU to a physical address used in cache memory. Both CAM and Static Random Access Memory (SRAM) share many similarities and functionalities. However, unlike SRAM, CAM has an ability to search within the memory against an input vector. Each memory bit in CAM has its own comparison circuit to determine whether a match is found; SRAM does not. This provides CAM a unique searching capability, with results in a larger area as a tradeoff. In addition to a larger overall area, energy consumption also increases because each cell performs comparison simultaneously. As the energy consumption increases, it becomes difficult to use in a portable system. Hence, to utilize the advantages of CAM in a mobile device, power reduction is a required task. The objective of this work is to investigate power reduction techniques and power-saving circuit architectures. The primary commercial application of CAMs todayis to classify and forward Internet protocol (IP) packets innetwork routers [7]–[12]. The power of any given system or device can be divided into dynamic and staticpower. Dynamic power consists of transistors switching activity and short-circuitedcurrent. Static power dissipation contributes by leakage current. The power usage of asystem can be modeled by the following equations [6]:

$$P_{Total} = P_{dynamic} + P_{static} = (P_{transistion} + P_{shortcircuit}) + P_{leakage}$$

$$P_{transistion} = \alpha * f_{clk} * \frac{CV^2}{2}$$

α = Activity factor

f_{clk} = Clock frequency

V = Power supply voltage

$\frac{CV^2}{2}$ = Energy dissipated for each transition

The transitional power of a device can be calculated based on its operatingfrequency, the probability of being active, load capacitance, and the power supply thatcharges the capacitors.
Dynamic power can be reduced enormously if power supply voltage isreduced. Additionally, lowering the clock frequency and lowering the amount ofactivity can also benefit reduce the amount of dynamic power consumption. Paradoxically, theclock speed has been increasing in many of today's applications. By lowering the powersupply, it can decrease the dynamic power consumption considerably with a tradeoff ofdecreasing the noise margin and performance. Similarly, P type and N type transistorsmay both be active simultaneously and in turn create a short-circuited scheme [2].
Many special varieties of CAM cells and architectures were proposed with theintention of total energy discount and maintained high assessment performance. Nonetheless, power and performance are instantly associated; when one wants to developefficiency, power additionally increases. At the same time, when power is diminished, performance also decreases. Accordingly, it stays a challenging assignment to scale back power andcontinue performance at the same time. Most of the prior works desirous about each, withtradeoffs.

II. Matchline Sensing Technics

This section reviews low power match line sensing techniques.

A. Conventional (Pre-Charge High) Matching Scheme

The traditional matching scheme involves pre-charging high to the match lines.In the NOR match line scheme, the match line stays excessive unless a mismatch happens,which attracts the in match line to the bottom. As a consequence, in the finish of the in match operation, logiclow shows a mismatch and an excessive suggest a match. Within the NAND in match line scheme,the match line pre-charges high, however when it is a matched word, the match line is pulledto the bottom or good judgment low. Consequently, it's regarded a suit when the in shape line showsa 0 and VDD otherwise.The power consumed for a mismatch is due when the rising side for pre-chargingand falling side for evaluation. Accordingly, the power consumed when a miss occurs is:

$P_{miss} = C_{ML} V^2_{DD} f$

C_{ML} represents the match line capacitance
V_{DD} represents the power supply
f represents the search operation frequency

The power consumption associated with a single match line depends on theprevious state. Consider there are n number of match lines in the CAM; the match linepower is then illustrated by the following equation:

$P_{ML} = nP_{miss} = nC_{ML}V^2_{DD}f$

If the previous state is a miss, it needs a pre-charge for the current stateequivalent to P_{miss}. At the same time, if the previous state is a match with the current comparison indicating a mismatch, then it also consumes the similar amount of poweras P_{miss}. If the previous state and the current state are equivalent, then the power consumed is negligible. This specifies the change of state is where power dissipated.

B. Low-Swing Schemes

The low-swing in match line scheme provides a method to decrease the power consumed within the suit line within the case of a suit. This method requires the suit line to significantly lower the voltage level; nevertheless, it is nonetheless ready to denote whether a match happens. With the riding voltage diminished, the equation for the match line may also be rewritten as:

$P_{ML} = nC_{ML}V_{DD}V_{MLSwing} f$

Where V^2_{DD} becomes $VDD_{VMLSwing}$

The major drawback to this scheme is the difficulty in producing a lower voltage drive to the match line without the use of an external power supply or buck converter. Instead, additional circuitries are added to the existing CAM architecture to reduce the voltage drive of the match line. A tank capacitor is added to drive the match line [3]. By inserting the tank capacitor, the match line voltage, if it were to pre-charge, would be:

$$V_{MLpre} = V_{DD} \frac{C_{\tan k}}{C_{ML} + C_{\tan k}}$$

Furthermore, since the match line voltage is reduced, it would not be capable ofdriving the match line to indicate a match (high). Hence, a sensing amplifier needs to beadded to the match line to amplify the signal. This scheme greatly reduces the drivingvoltage in the match line, at the price of increasing the overall area and the complexity ofthe circuit.

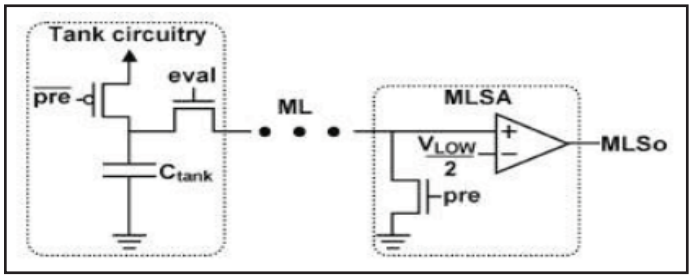

Fig. 2: Low-Swing Match Line Scheme Configuration [4]

C. Selective Pre-Charge Scheme

The selective pre-charge scheme is a slightly different method of reducing thematch line powers. The method of reducing the match line power is to selectively precharge certain match lines evaluated as having the potential of matching [4]. The Selectiveprecharge performs the match operation on the first few bits of a word. Once all the bitsin a word matched, the match line is charged and compared with the rest of the bits. Forthe first few bits not

matched, the match line is not pre-charged; hence, power is saved.This method works very well when data distributions are uniformly distributed. However,the power would be equivalent to an ordinary pre-charge scheme when all the first fewbits of the word are identical. A simple implementation of the selective pre-chargescheme is shown below:

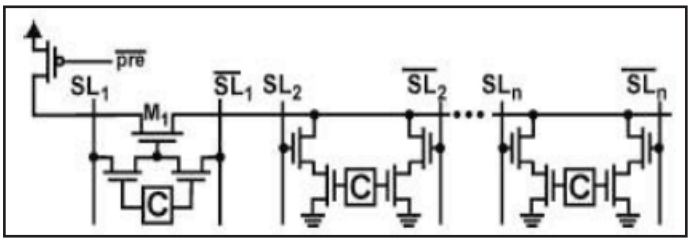

Fig. 3: Selective Pre-Charge Transistors Configuration [4]

D. Current Race

The Current Race scheme is another technique for reducing the power consumedin the match line. In this scheme, the match line pre-charges low and evaluates the matchline states by charging the match line with a current I_{ML} supplied by a current source [5]. Theconfiguration is shown in fig. 4.

In the pre-charge phase, the match line is pulled down to ground when mlpre ishigh. During the evaluation phase, mlpre is low and en' connects the current source to thematch line. If there is a match, then the match line charges linearly to a high voltage. Thisturns on M_{sense} with the half-latch outputting M_{LSO} high as the indication of a match. In the case of a mismatch, the match line charges to a voltage of $\frac{I_{ML}*R_{ML}}{N}$.

N represents the number of bits that are a mismatch (pulls to the ground) and R_{ML} indicates the resistance for the transistor that pulls the match line to ground. The M_{sense} transistor trips the latch with a threshold of V_{TH}. In the case of matching, the matchline is charged aboveV_{TH}, pulling the input of the half-latch to low and output M_{LSO} to high.

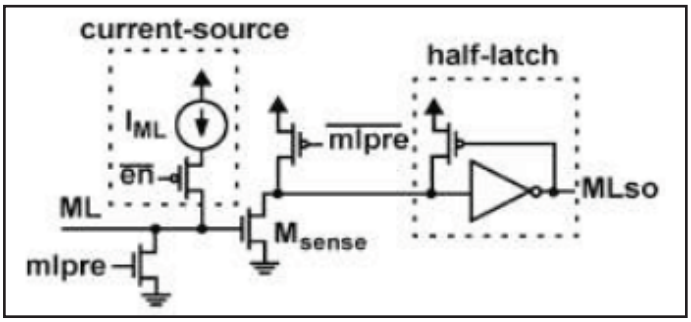

Fig. 4: Current Race Transistor Configuration [4]

For amismatch, the match line has less voltage and leaves the latch with the initial state. The power consumption is very similar to the case of low-swing scheme, except the matchline voltage is slightly above V_{TH}. This is also the case when a mismatch occurs. Hence, the power consumed using this scheme is:

$$P_{ML} = nC_{ML}V_{DD}V_{tn}f$$

D. Pipelining Scheme

In this scheme a CAM word is broken into several segments and each segment is evaluated serially in pipelined fashion, only the words that match a segment can proceed with the next segment search [6]. The major disadvantage of this technique is increased latency and area but in terms of saving power it is good.

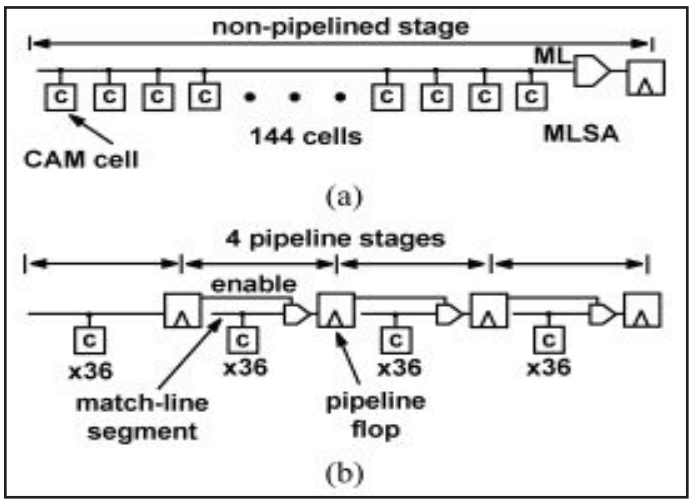

Fig. 5 Pipe Lining Scheme

III. Low Power Cam Architectures

In this section, we review architectural techniques for saving power.

A. Bank-Selection Scheme

Fig. 6 provides a block diagram of a simplified bank-selection scheme. Two extra data bits, called bank-select bits, partition the CAM into fourblocks. When storing data, the bank-select bits determine intowhich of the four blocks to store the data. When searching data,the bank-select bits determine which one of the four blocks to activate and search. The decoder accomplishes the selection byproviding enable signals to each block. In the example, the bank-select bits are 10 which selects bank 2.

In the original preclassification schemes, this architecture wasused to reduce area by sharing the comparison circuitry betweenblocks. Although the blocks in Fig. 6 are shown as physicallyseparate, they can be arranged such that words from differentblocks are adjacent. Since only one of four blocks is active at anytime, only 1/4 of the comparison circuitry is necessary comparedto the case with no bank selection, thus saving area. Instead of saving area, recent bank selection schemes aimto reduce power [3]. Bank selection reduces overall powerconsumption in proportion to the number of blocks. Thus, usingfour blocks ideally reduces the power consumption by 75%compared to a CAM without bank selection.

The major drawback of bank selection is the problem of bankoverflow. Since, in a CAM, there are many more input combinations than storage locations, the storage of a bank can quicklyoverflow. Take, for example, a CAM with 72-bit words (andan additional bank-select bit) and 32K entries divided into twobanks with 16K entries. While each bank has 16K locations,there are actually 2 possible entries per bank.

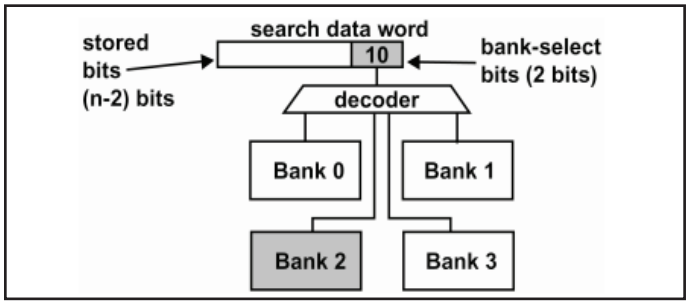

Fig. 6: Simplified Diagram of a Bank-Selection Scheme. The bank-Selection Scheme Partitions the CAM and Shuts off Unneeded Banks

Thus, it canoften occur that there are more entries than can fit in the assignedbank. This overflow condition requires extra circuitry and forcesmultiple banks to be activated at once, decreasing the savings inpower. To avoid overflow, an external mechanism can balancethe data in the banks by periodically re-partitioning the banks.

B. Static Divided Match Line Architecture

The CAM circuit consumes most of the power for comparison because it performs large number of comparisons to find all valid data that stored in CAM per data searching operation.

In order to reduce the comparison power consumption in this architecture as shown in fig. 7, the searching operation divides the comparison process in to two steps; first partial bits among n-bits are selected for comparison process. If these partial bits of the input data mismatch those of stored data, then the input data mismatches the stored data other wise, match or mismatch information is determined by the comparison result of second comparison process. This scheme effectively reduces the number of comparisons and thus reduces power consumption [13]. Even though the search operation is separated in to two comparison processes,however these two processes are performed in parallel which improves searching performance

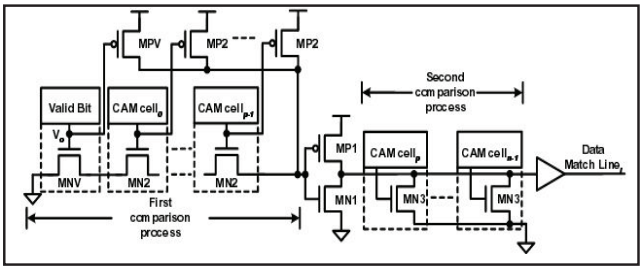

Fig. 7: Static Divided Match Line Architecture

C. Butterfly ML TCAM

The butterfly match-line (ML) TCAM scheme is proposed making use of pseudo-footless clock data precharge dynamic (PF-CDPD) structure. It's related the every pipelined stage is in the butterfly association structure which is utilized for minimize the power consumption and search time. The power utilization on the search line is lowered without any search time overhead. A noise-tolerant match-line (ML) scheme with XOR-based conditional keeper is introduced to decrease the power consumption and search time. With the exact finish of the target to reduce the search time overhead caused through butterfly connection variation the XOR-based conditional keeper system can reducedelay of critical path of the match-line.

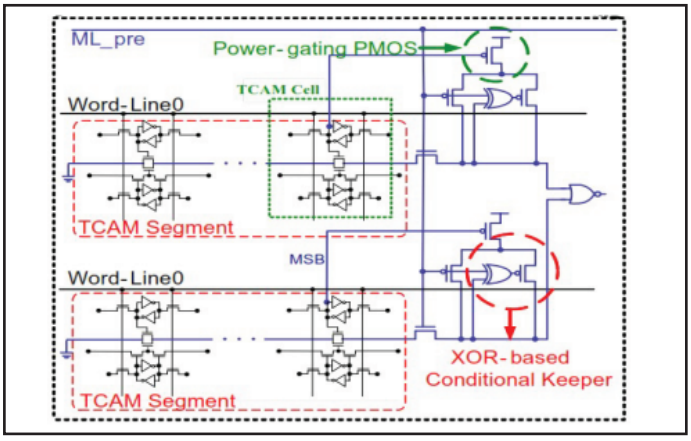

Fig. 8: Butterfly ML TCAM

Fig. 8 shows the butterfly connectionstructure. The two CAM segments are related in the butterfly connection structure. The twoCAM segments are linked using two input NOR-gate, and controlled signal of next stage isgenerated by the two input NOR-gate output.

D. Master-slave Match Line Design

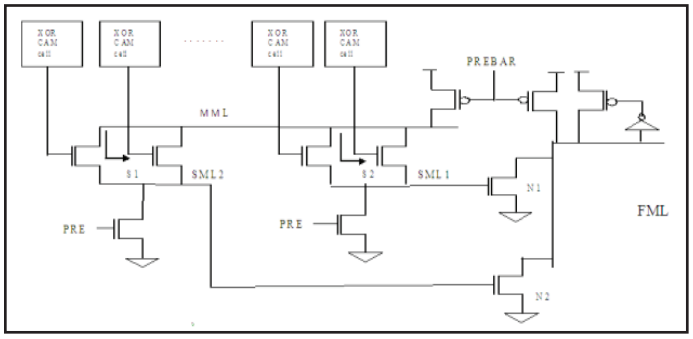

Fig. 9: CAM using MSML Architecture

The fundamental notion in the back of this design is cost fill up minimization process. This will likely lower the match Line power consumption. In this design whole CAM word is split into quantity of segments. Each and every segment is offered with a Slave match Line. Right here the power consumption across in match Line is decreased by way of reducing the voltage swing on matches Line throughout charging and discharging of match Line. When any miss match occurs in someone of the CAM cell, then the cost throughout the match Line is dispensed to the Slave match Line to which the miss match CAM cell belongs. Then, for the duration of the subsequent precharge cycle, the match Line is charged to the VDD, however the voltage swing reduces as the match Line holds intermediate voltage worth depending on the number of mismatched segments. By using cost sharing, the Slave in shape strains will likely be charged to distinctive voltage worth. This will turn on the pull down transistor to which the final matchLine is hooked up. Then the final matchLine will likely be discharged to ground when a mismatch happens. The circuit for the MSML design is given in the fig. 7

IV. Conclusion

In this paper, we have surveyed CAM circuits and architectures, with an emphasis on high-ability CAM. First, weinspired our dialogue by way of displaying how CAMs will also be utilizedto packet forwarding in network routers. We have explored the conventional precharge-high scheme for sensingthe matchline, as well as a couple of editions that save matchlinepower including low-swing sensing, the current-race scheme,selective pre charge and pipelining.Finally atthe architectural stage, we have reviewed four architectures forreducing CAM power, specifically Master-Slave Match line architecturereduces thepower consumption veryeffectively when compared to other available techniques.

References

[1] K. Pagiamtzis, A. Sheikholeslami,"Content-addressable memory (CAM)circuits and architectures: a tutorial and survey," Solid-State Circuits, IEEE Journal of, Vol. 41, pp. 712-727, 2006.

[2] R. Ahmadi,"A Low Power Sense Amplifier Flip-Flop with BalancedRise/Fall Delay," In Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEEInternational Conference on, 2006, pp. 1292-1295.

[3] G. Kasai, Y. Takarabe, K. Furumi, M. Yoneda,"200 MHz/200 MSPS3.2 W at 1.5 V Vdd, 9.4 Mbits ternary CAM with new charge injectionmatch detect circuits and bank selection scheme," In Proc. IEEE CustomIntegrated Circuits Conf. (CICC), 2003, pp. 387–390.

[4] C. A. Zukowski, S.-Y. Wang,"Use of selective precharge for lowpower content-addressable memories," In Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), Vol. 3, 1997, pp. 1788–1791

[5] I. Arsovski, T. Chandler, A. Sheikholeslami,"A ternary contentaddressable memory (TCAM) based on 4T static storage and including a current-race sensing scheme," IEEE J. Solid-State Circuits, Vol. 38, No. 1, pp. 155–158, Jan. 2003.

[6] K. Pagiamtzis, A. Sheikholeslami,"Pipelined match-lines and hierarchical search-lines for low-power content-addressable memories," In Proc. IEEE Custom Integrated Circuits Conf. (CICC), 2003, pp. 383–386.

[8] Y. Taur, T. H. Ning,"Fundamentals of modernVLSI Devices", New York:Cambridge Univ. Press, 1998, Ch-2, pp. 94-95

[9] T.-B. Pei, C. Zukowski,"VLSI implementation of routing tables:tries and CAMs," In Proc. IEEE INFOCOM, Vol. 2, 1991, pp. 515–524.

[10] "Putting routing tables in silicon," IEEE Network Mag., Vol. 6, No.1, pp. 42–50, Jan. 1992.

[11] G. Qin, S. Ata, I. Oka, C. Fujiwara,"Effective bit selection methodsfor improving performance of packet classifications on IP routers," InProc. IEEE GLOBECOM, Vol. 2, 2002, pp. 2350–2354.

[12] H. J. Chao,"Next generation routers," Proc. IEEE, Vol. 90, No. 9, pp.1518–1558, Sep. 2002.

[13] C. Kuo-Hsing, W. Chia-Hung, J. Shu-Yu,"Static divided word matching line for low-power Content Addressable Memory design," In Circuits and Systems, 2004. ISCAS '04.Proceedings of the 2004 International Symposium on, 2004, pp. II-629-32, Vol. 2.