A Review on Performance of 6 Transistors and Schmitt Trigger based 10 Transistors Static Random Access Memory Cell

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Abstract
In this paper, the read and write operation of 6 transistors based SRAM (Static Random Access Memory) cell and Schmitt trigger based 10 transistors SRAM cell topologies for low voltage and low area applications are studied and simulated. The robust Schmitt trigger based 10 transistors memory cell exhibits built-in process variation tolerance that gives better immunity to noise and other performance parameters. The tool used for simulation purpose is IC station by Mentor Graphics using TSMC 180nm CMOS technology.

Keywords
Read and Write Operation, 6T SRAM Cell, Schmitt Trigger (ST) based SRAM Cell.

I. Introduction

According to International Technology Roadmap for Semiconductors (ITRS), Memory is expected to occupy about 90% of the chip area in 2013. As the semiconductor process is scaled down, the thickness of gate oxide becomes thinner in order to decrease the core power-supply voltage (VDD) [1]. SRAM cell read and write stability is major concern in CMOS technologies due to the supply voltage and technology scaling. In low power VLSI, Stability degrades due to technology scaling and fluctuations in process parameters that is oxide thickness, diffusion depth and density of impurity concentration [2-3] etc.

The Schmitt Trigger is a comparator that incorporates positive feedback. The circuit is named a "trigger" because the output retains its value until the input changes sufficiently to trigger a change. Schmitt trigger is used to modulate the switching threshold of an inverter depending on the direction of the input transition. The output state depends upon the input level and will change only as the input crosses a predefined circuit threshold. Therefore Schmitt Triggers are bi-stable networks that are widely used to enhance immunity of circuits to noise and disturbances [4].

II. The Conventional 6T SRAM Cell

The conventional 6T SRAM cell is shown in fig. 1. It consists of two cross-coupled feedback CMOS inverters (P1, N1) and (P2, N2) with two NMOS access transistors which connect the bit (BL) and bit-bar (BLB) line.

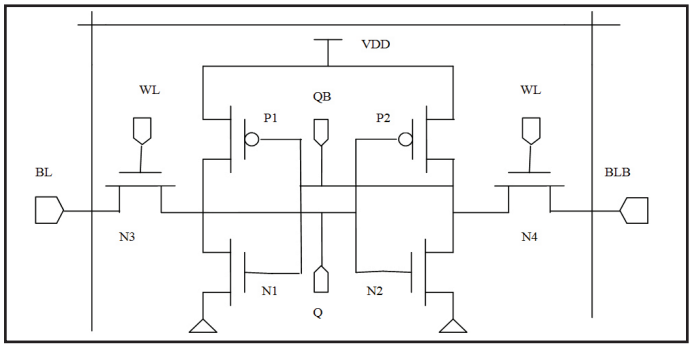

Fig. 1: The 6 Transistors SRAM cell.

These two lines connect this storage cell to the external device. The access transistors are activated by word line (WL) which is selected by the row decoder address. The bit (BL) and bit-bar (BLB) lines are selected by the column decoder address. Then a particular cell is selected by the combination of row and column decoder address. This makes a complete single bit 6T SRAM cell. In most of SRAMs, the word lines are made from poly-silicon while the bit lines are metal. Due to large number of rows and column in a memory array, it makes a big and wide memory.

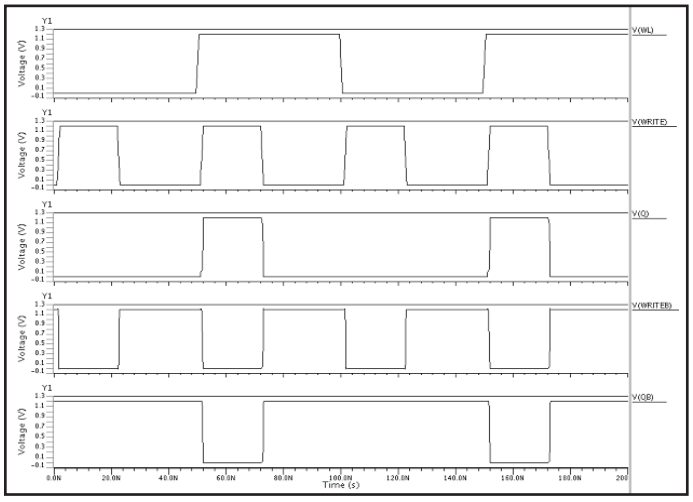

Fig. 2: The Write Waveform of 6 Transistors based SRAM Cell

Thus the word and bit lines run all through the cell. So a large part of delay is due to charging and discharging of these lines. This leads to power dissipation, leakage and stability problems. Therefore Careful transistors sizing is also required to ensure a stable read and write operation [4]. The transistor sizing constraints must be taken into consideration for a successful write operation such that the cell should allow modification of the stored information during the data-write phase [6].

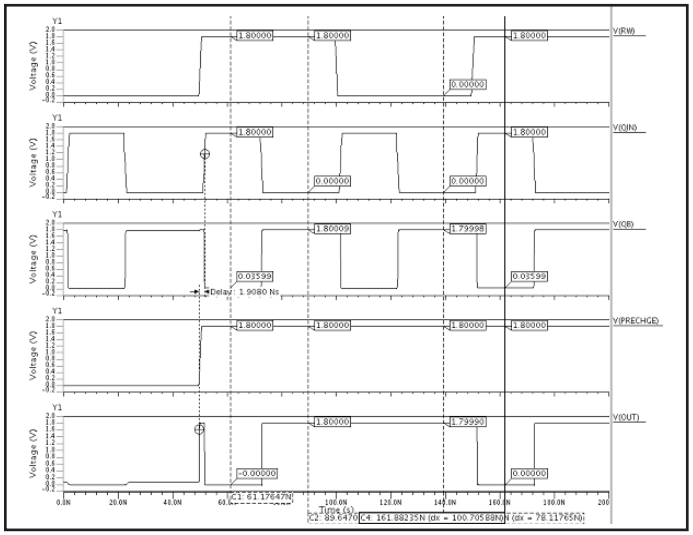

Fig. 3: The Read Waveform of 6 Transistors based SRAM cell

A. The Existing Schmitt Trigger based 10 transistors SRAM Cell

The existing Schmitt Trigger circuit consists of three pMOS devices P1, P2, P3 and three nMOS devices N1,N2, N3 as shown in Figure 4 [5]. Schmitt Trigger circuit has two different high-to-low (VH) and low-to-high transition (VL) threshold voltages which make the circuit to have better noise immunity than the inverter. When output signal is pulled low as input signal exceeds VH. Similarly, when the output signal is pulled up as input signal is lower than VL. Hence, the noise immunity of the existing ST circuit is better than that of inverter. Initially input voltage (VIN) in Fig. 4 is equal to 0V, to turn on the two stacked pMOS transistors P1 and P2. Hence output voltage (VOUT) will be equal to VDD.

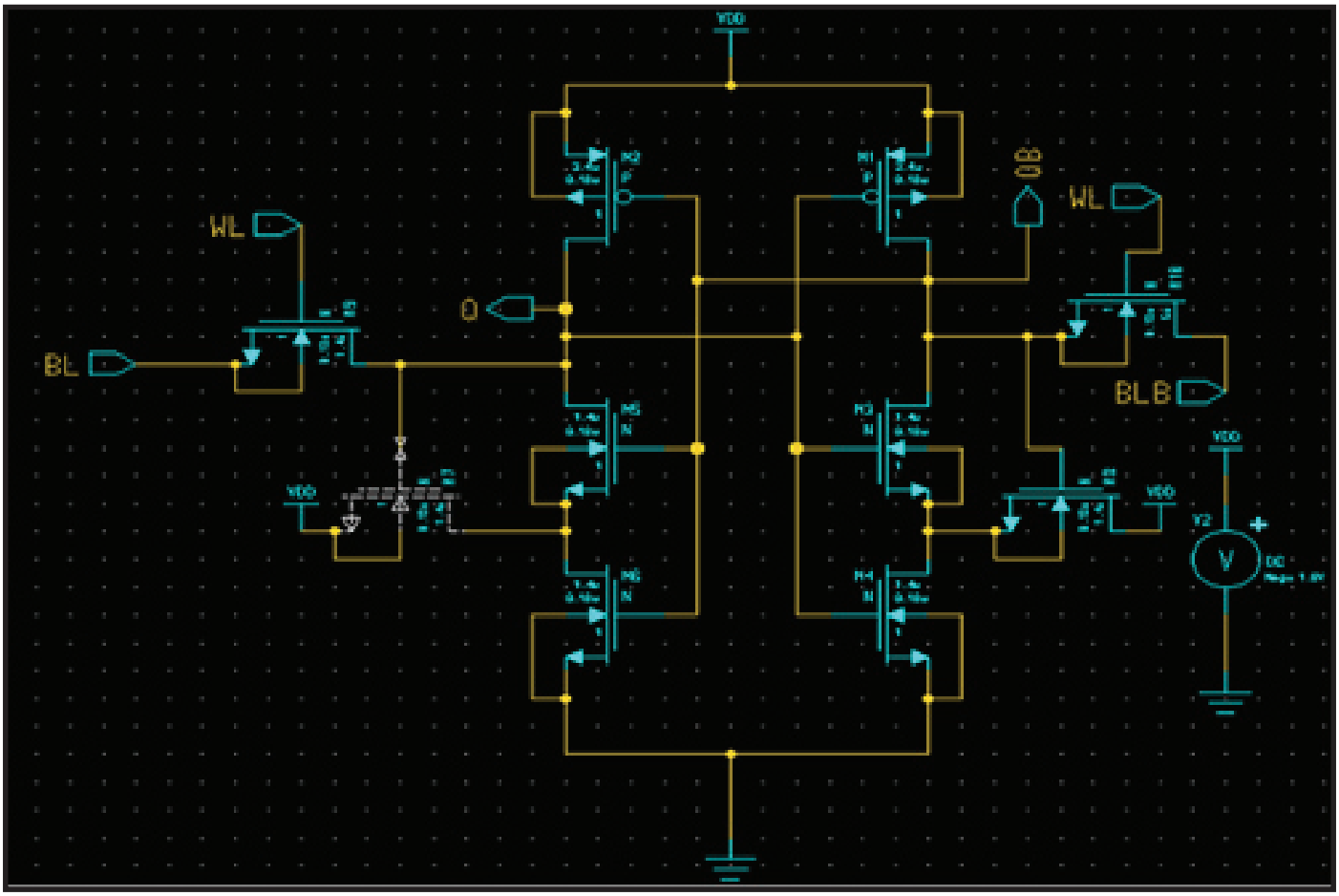

Fig. 4: Existing Schmitt Trigger Circuit

When VIN rises to threshold voltage of nMOS (VTN), N2 will turn on but N1 remains off since N3 is on and hence source voltage of N1 becomes VDD - VTN. Now N2 and N3 are forming an inverting nMOS amplifier. Thus the source voltage of N1 is falling with increasing VIN. When source voltage of N1 drops to VTN, N1 becomes on. Here both N1 and N2 are on, causing VOUT to be driven to 0V rapidly so that N3 becomes off. When VIN falls below the threshold voltage of pMOS (|VTP|), P1 will turn on but P2 remains off since P3 is on, forcing the source voltage of P2 to 0V. Now P1 and P3 are forming an inverting pMOS amplifier. Thus source voltage of P2 is rising with decreasing VIN. When source voltage of P2 rises to |VTP |, P2 becomes on. VOUT approaches to VDD rapidly as P1 and P2 are on to drive P3 off.

In order to find a solution for the conflicting read versus write operation design requirement in the 6T SRAM Cell, Schmitt Trigger principle is applied for the cross coupled inverter pair. A Schmitt trigger increases or decreases the switching threshold of an inverter depending on the direction of the input transition [7].

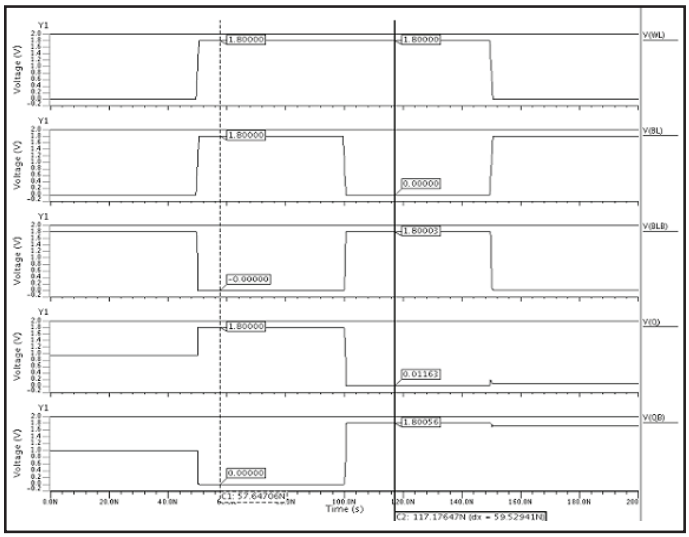

Fig. 5: Schmitt Trigger Based SRAM Cell Write Operation.

In this, a feedback mechanism in pull down path is used. During a read Operation (Q ='0' and QB ='1'), the voltage on Q rises due to voltage divider action between access transistor and pull

down transistor. If this voltage becomes higher than the switching threshold of the other inverter, the content of the cell can destroy. This result read failure event [8].

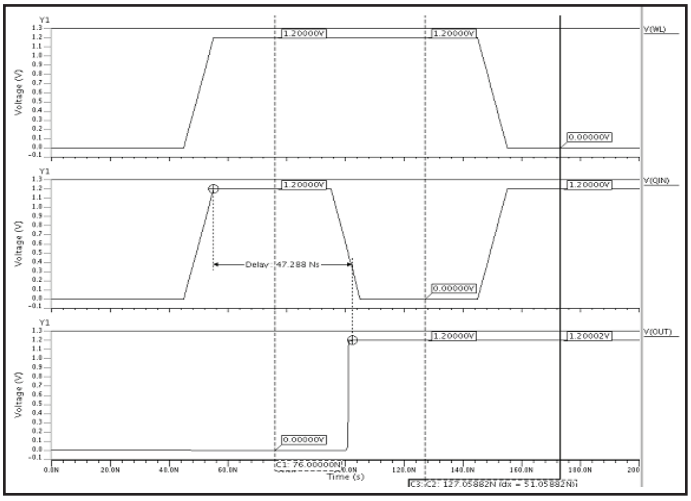

Fig. 6: Schmitt Trigger Based SRAM Cell Read Operation

In order to avoid read failure event, this topology is used. In this topology, transistor N5 and N6 raises the switching threshold of source voltage of transistor N4. Thus the feedback transistor tries to preserve the logic'1' at the output of cell [5].

III. Conclusion

Lowering the supply voltage is an effective way to achieve low power operation. In the work, evaluation of the 6 transistors and Schmitt trigger based SRAM cell were be done. The read and write waveforms of both topologies are analyzed at low voltage. The built-in feedback mechanism in the ST bit cell can be effective proposal for process tolerant, low voltage SRAM operation in future nano- scaled technologies.

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