Design and Analysis of Novel Digital Pulse Width Modulator Architecture

[1]Shubham Gupta, [2]Dr. Vineeta Saxena Nigam
[1,2]Dept. of ECE, UIT RGPV, Bhopal, MP, India

Abstract
The keep coming advantages of digital techniques over analog has led to increasing use of digital equipment in modern world. Among such equipment Digital Pulse Width Modulator Architectures has unique place. These are used for controlling magnitude of Voltage/ Current with fine accuracy. The paper describes high resolution digital pulse width modulator architecture with decreased time resolution by using Field Programmable Gate Arrays (FPGA). The proposed architecture uses Fine Phase shifting Mechanism of On-Board DCM present in FPGA Devices. Moreover the proposed architecture has reduced time resolution, power and delay as compared with other pulse width modulator architecture.

Keywords
FPGA, DCM, Fine Phase shifting, VHDL.

I. Introduction

In recent time the world is full of electronic devices. The working of these devices is different based on their usage. The devices which are used for control system has made a significant influence in human lifestyle. These control devices are uses in many electronic and electrical appliances such as HDTV, Remote control mechanisms etc. The novel equipment used in control techniques is Pulse Width Modulator (PWM). As it's name it is clear that Pulse Width Modulators are the devices which are used for varying width of pulse. The two important domains in which Pulse Width Modulator are commercially available [8-9]. These domains are:

1) Analog and
2) Digital.

Although there are many Analog PWM architectures available, Digital PWM is increasingly becoming popular. Based on various architectures and realizations of the key building blocks, the High Resolution high-frequency digital pulse width modulators (DPWM) [5-6, 15], in comparison to analog pulse width modulator offer the advantages of:

Lower sensitivity to parameter variations: Due to quantization and encoding processes involved with Digital signal, these signal shows lower sensitivity to parameter variation [4]. A device showing lower sensitivity to parameter variation is thus said to be least affected by noise. Digital signal after quantization has number of levels associated with it and the effect of ringing oscillation is greatly reduced due to this.

Programmability: Digital devices can be easily programmed using any of the coding language like VHDL, Verilog etc. Using these programming languages user can opt any tool like Xilinx, Quartus II containing the library of respective programming language [7].

Removal of external analog components, without compromising the performance, simplicity or cost: Digital devices do not require any analog component like resistors, capacitors and inductors for their operation. These devices are composed of either combinational logic like gates, multiplexer etc. or sequential logic element like SR flip-flop, counter etc. as basic building block [10]. For implementing the functionality of devices composed of them, it is necessary to study the individual behavior of these basic building blocks.

On the contrary, analog control is free from terms like resolution and sampling without which digital control is impossible. Thus, the digital control apart from providing almost noise free environment and advantages listed above has added ambiguities in the form of limited resolution and added delays due to sampling and other processing technique leading to degraded accuracy [11-12].

II. Proposed Architecture

The main element of proposed architecture is DCM, one of the features present in almost every on board FPGA. DCM allows solution to following clocking issues: i) Multiplication and division of input frequency: It thus allows synthesis of variety of frequency by using some multiplication and division operation. ii) Clock Conditioning: This feature allows clean output frequency with 50% duty cycle. iii) Phase Shifting Mechanism: Input clock can be phase shifted by either fixed fraction or fine increments.

The DPWM architecture [1-3] uses phase shifting mechanism of DCM. The DCM allows four different kinds of phase shifting mechanism. Each of these types may be used independently, or in combination with other phase shifting modes.

1. Half-Period Phase Shifted Outputs: It generates output clock with 50% duty cycle. A pair of outputs provides a rising edge at 0° and 180° phase shift—or, at the beginning and half-period points during the clock period.
2. Quadrant Phase Shifted Outputs: Clock outputs are generated with phase shift of 0° (CLK0), 90° (CLK90), 180° (CLK180), and 270° (CLK270), with option of adjustable duty-cycle.
3. Fixed Fine Phase Shifting: In this mechanism DCM generates clock outputs with a resolution of 1/256th of a clock cycle.
4. Dynamic Fine Phase Shifting: There is little variation in this mechanism with respect to Fixed Fine Phase Shifting mechanism. In this clock outputs are generated for within the FPGA application, again with a resolution of 1/256th of a clock cycle.

The DCM provides additional controls over clock using fine phase shifting [13-14]. Fine-phase adjustment affects DCM output clocks simultaneously. The fine phase shift capability requires the DCM's DLL functional unit. Consequently, clock feedback via the CLKFB input is required.

Physically, the fine phase shift control adjusts the phase relationship between the rising edges of the CLKIN and CLKFB inputs. The net effect, however, is the all DCM outputs are phase shifted with relation to the CLKIN input.

By default, fine phase shifting is disabled (CLKOUT_PHASE_SHIFT=NONE), meaning that the clock outputs are phase aligned with CLKIN. In this case, there is no skew between the input clock, CLKIN, and the feedback clock, measured at the appropriate feedback point. When fine phase shifting is enabled, the output clock edges can be phase shifted so that they are advanced or are retarded compared to the CLKIN input, as shown in Figure.

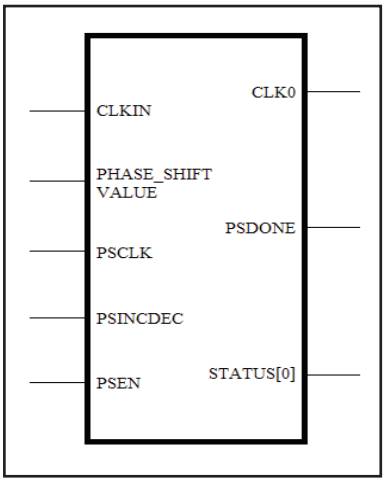

Fig. 1: DCM with Fine Phase Shift Control

There are two fine phase shift modes as described below. Both are commonly used in high speed data communications applications.

1. **Fixed Fine Phase Shift** mode sets the phase shift at the time of design. The phase shift value cannot be changed by the application as it is loaded during the FPGA configuration process.
2. **Dynamic Fine Phase Shift** mode has some phase shift value initially, similar to Fixed Fine Phase Shift, which is set during FPGA design configuration time. Nevertheless, the phase shift can be changed by after the DCM's LOCKED output goes to high state.

Fixed Fine Phase Shifting

In Fixed Fine Phase Shift, the phase shift value is selected at time of the design and set during the FPGA configuration process. The change in phase shift not done between run time.

To control this mode 2 properties are use. The value of CLKOUT_PHASE_SHIFT is set FIXED, and the PHASE_SHIFT controls the phase shift. If PHASE_SHIFT value is is 0, then the output clocks and the CLKIN input are phase aligned, as shown in Figure 1. If PHASE_SHIFT is a negative integer, then the clock output(s) are phase shifted before CLKIN. If PHASE_SHIFT is a positive integer, then the clock output(s) are phase shifted after CLKIN.

Fixed Fine Phase Shift Range

The PHASE_SHIFT has integer value, ranging from –255 to +255. However, the actual limits may be lower depending on the CLKIN input frequency.

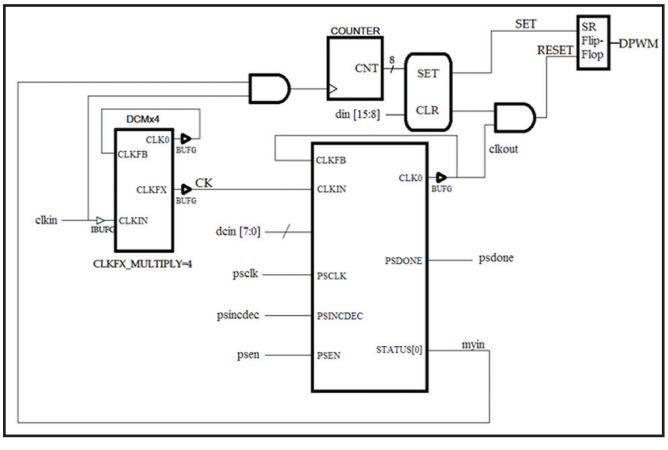

Fig. 2 proposed Architecture of DPWM.

The minimum and maximum limit of the PHASE_SHIFT attribute depends on two values.

1. The period of the CLKIN input, TCLKIN, measured in nanoseconds.
2. The value of the FINE_SHIFT_RANGE specification for the Spartan-3 device and speed grade, found in the Spartan-3 Data Sheet. FINE_SHIFT_RANGE is the total delay achievable by the phase shift delay line, which is a function of the number of delay taps used in the circuit. The actual delay line may be longer than FINE_SHIFT_RANGE, but only the delay up to FINE_SHIFT_RANGE is guaranteed.

Other Design Considerations

In Fixed Phase Shift mode, the Dynamic Phase Shift control inputs must be tied to GND, which DCM Wizard does automatically.

III. Proposed Modified Architecture

The Proposed architecture uses two DCM, counter, comparator, set reset flip flop and set of AND gate for implementation of digital pulse width modulation. The first DCM is used for clock multiplication by some factor. The second DCM is used for providing fixed fine phase shifting as discussed above. For using DCM in fixed phase shifting, psincdec, psen, psclk act as input while psdone, status act as output. Moreover, a feedback of clock output is provided at the input in both the DCM. It is done to obtain more stable output frequency. The fixed fine phase mechanism is operated in FPGA is explained and shown in figure below.

The fixed fine phase shift operation of DCM is based on psclk i.e. phase shift clock which is used as input by the internal linear counter inside DCM. psen as shown in figure below is phase shift enable which is used to acknowledge DCM that a phase shift operation is enabled. It is to clear that for fixed fine phase shifting operation it must be enabled for one clock cycle. psincdec is nothing but acknowledgment to DCM that whether a phase shift increment operation is enabled or decrement operation. If shift increment operation needs to done then, psincdec should be kept high for same duration as psen is enabled. Moreover, if decrement operation needs to done then psincdec should be kept low for same duration as psen is enabled. When the linear internal counter embedded in FPGA is finished with the phase shift operation based on phase_shift value, the psdone is enabled for one clock cycle of psclk indicating that internal linear counter is finished with the phase shift operation.

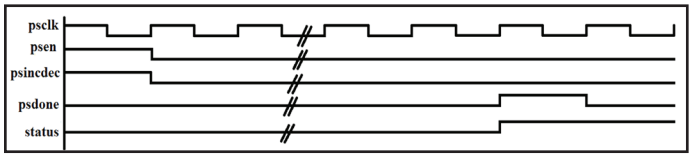

Fig. 3: Fine Phase Shift Based DCM Operation

Moreover, the status signal goes high as well indicating that phase shift operation is finished.

Counter and comparator as shown in the above architecture are used to govern the on time of PWM waveform. Moreover, input clock to counter is provided by AND operation of status signal and clock input to second DCM. This is done to ensure that clock start counting only when DCM is finished with fine phase shift operation. Therefore, a modified clock is provided to the counter. This is done to ensure that counter starts counting at the proper time. Otherwise, the counter will state counting much before resulting in degraded performance of digital pulse width modulator architecture. This modified clock is generated with the help of

AND gate. As it is clear that counter must start counting only when the DCM is finished with the fixed fine phase shifting operation. As discussed above when the DCM is finished with the phase shift operation it generates status terminal to high. Therefore, this status signal is AND operated with input clock to obtain modified clock necessary for counter operation. Data input is fed at one of the input of the comparator. This comparator compares the provided data input with the value as provided by the counter to the other terminal of the comparator. Whenever the counter count reaches to the same value provided to comparator as data input then, comparator output is set. The comparator output is low as long as the counter count is less than data input provided to comparator. The comparator output is fed to RS flip flop to set/ reset the generated pulse width modulated output.

IV. Xilinx Implementation

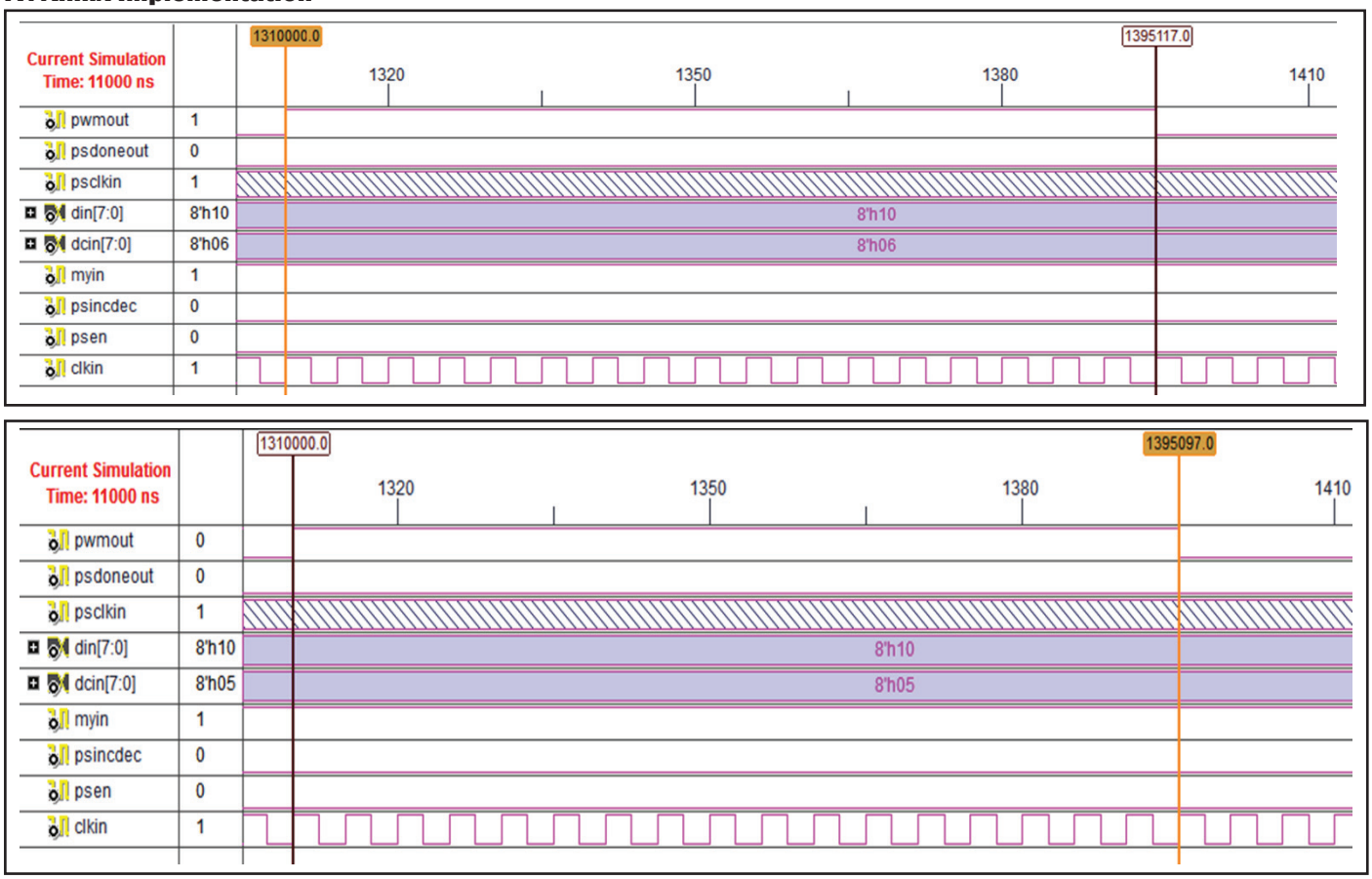

Fig. 4: DCM based DPWM Operation

Xilinx tool allows both synthesis and simulation capabilities. Synthesis in Xilinx result in generation of RTL schematic. While simulation results in generation of waveform governing the functionality of implemented design. The synthesized result contain information regarding number of slices, number of slice flip flops, number of 4 input LUTs, number of bonded IOBs, number of GCLKs, number of DCMs being used in proposed HRDPWM with. Simulation result contain the information regarding desired output in respect with the applied input. The proposed architecture is simulated in ISE simulator. From block diagram as shown above it is clear that there are two DCMs used foe design implementation. One DCM is used for clock multiplication while other DCM is used for generating phase shifted output in accordance with the 8 bit input applied to DCM. From the above waveform it is clear that the proposed architecture act as pulse width modulator only after the status signal is set. Before the status signal is set, DCM performs the fine phase shifting mechanism to provide fine phase shifted output. To overcome clock mismatch applied to counter AND gate is used with status signal as one input. The counter used is 8 bit counter to count number of clock pulses. The counter count is fed to 8 bit comparator which compares it with 8 bit input provided to it.

The comparator output is used to set ON i.e. govern the ON time of the PWM output while the phase shifted output is used to govern the OFF time of PWM output.

V. Results

The proposed architecture is implemented in Xilinx using General purpose product category, Spartan 3E family, XC3S250E device having TQ144 package. Out of available speed of -5 and -4, the architecture used speed of -4. Table1 shows synthesis result for proposed architecture as obtained with Xilinx tool. The comparision result from other architecture is clearly shown in table.

Table 1: Synthesis Result for Proposed Architecture as compared with other architecture

Logic Utilization	[2]	Proposed Architecture
Number of Slice Flip Flops	22	9
Number of 4 input LUTs	14	12
Logic Distribution Number of occupied Slices	25	11
Number of Slices containing only related logic	25	11

Number of Slices containing unrelated logic	0	0
Total number of 4 input LUTs	21	19
Number used as logic	14	12
Number used as route-thru	7	7
Number of bonded IOBs	13	15
Number of GCLKs	6	3
Number of DCMs	3	2
Total equivalent gate count for Design	21353	14219

Table 1 shows the results obtained after the synthesis of proposed architecture and other HRDPWM Architecture in Xilinx tool . From Table1 it is clear that number of slices, number of slice Flip Flops and Number of 4 input LUTs have reduced significantly. It is due to reduced logic distribution in proposed architecture. Altough, there is increase in number of bonded IOBs but there is noted decrease in Number of GCLKs and DCMs. The net result is therefore decrease in total equivalent gate count for proposed architecture.

Power consumption of proposed architecture as carried out in XPower tool in shown in Table 2.

Table 2: Estimated Power for Proposed Architecture as compared with other architecture

	[13]		Proposed Modification
Nominal Total Power (W)	0.914	0.662	0.453
Worst case Total Power (W)	1.181	0.952	0.503

The estimated power consumption for proposed architecture is tabulated as shown in Table2. The estimated power for proposed architecture is compared with other architecture. Clearly, it is seen that there is significant reduction in the estimated power for proposed architecture. This reduction in power can be attributed to reduced total equivalent gate count for Design.

From above waveform it is clear that PWM output goes to logic low level for two consecutive control input word of 0000101000000110 and 0000101000000101 at 1395117 ps and 1395097 ps respectively. The difference between these times gives the time resolution for the architecture. Thus, the minimum time resolution that is obtained comes out to be 20 ps.

VI. Conclusion

The proposed architecture is novel approach towards implementation of digital pulse width modulator architecture. Proposed architecture is well tested and analyzed in Xilinx. The architecture and its various associated parameter has been thoroughly examined. With this proposed architecture time resolution as low as 20ps is made possible. It is to be noted that the architecture enabled equivalent gate count as low as possible to 14219. The power consumption by architecture is reduced to 0.503 W which is added advantage to proposed architecture. The architecture is well suited for use in controlling the speed of stepper motor to more fine levels. Moreover, there can be further advancement in lowering the time resolution of digital pulse width modulator.

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