Evaluation of Costas Loop for BPSK Demodulation

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Abstract
The paper presents the design and implementation of Costas loop in a binary phase-shift-keying (BPSK) demodulation scheme. The signal of interest is a 10KHz carrier BPSK modulated by 4 Kbps data, with a sampling frequency of 10MHz set at the receiver. The Costas loop compensates for frequency and phase errors caused by various sources like clock drifts, Doppler shift and bit-time errors. A novel architecture for NCO (Numerically Controlled Oscillator) has been used in the evaluation of the Costas loop. The simulation has been carried out using MATLAB Simulink and Modelsim PE and each module is verified for its working.

Keywords
BPSK, NCO, Costas Loop, PLL (Phase-Locked Loop), Filter, Phase and Frequency Offsets.

I. Introduction

In coherent demodulation, a reference carrier signal is required whose phase and frequency are in synchronism with carrier used for modulation purpose. This allows the demodulator to make use of all available information in the received signal, and thus can provide maximum-likelihood detection [1]; i.e., an ideal coherent demodulator yields the minimum possible probability of error. However the reference carrier may not be available easily and hence has to be recovered from the received signal, which is indeed difficult procedure.

Carrier synchronization can be achieved by sending a pilot tone before message signals. Because the pilot tone has a strong spectral line at the carrier frequency, the receiver can easily lock on it and generates a local coherent carrier. However, this requires extra transmission bandwidth. Carrier synchronization also can be achieved with a carrier recovery circuit which extracts the phase and frequency information from the noisy received signal and use it to generate a clean sinusoidal reference signal.

Designs for PLL's (Phase-Locked Loops) can be broadly categorized as follows [2]: squaring loops, Costas loops, decision directed feedback loops. Among them Costas loop is the most popular because of its ease of implementation compared to squaring device and ability to provide rapid carrier recovery as against the decision-directed loops which make use of initial training sequence.

A Costas loop is a type of phase-locked loop that is used for carrier synchronization in a receiver when the modulation is BPSK. The Costas-loop relies on feedback concept for its operation. It offers an inherent ability to self-correct the phase and frequency of the recovered carrier and its implementation is not more complicated than the squaring technique and hence the Costa' s loop is the preferred technique for PSK demodulation over the squaring loop. The primary application of Costas loops is in wireless receivers. Its advantage over the PLL-based detectors is that at small deviations the Costas loop error voltage is sin $(2(\theta_i-\theta_f))$ vs. sin $(\theta_i-\theta_f)$. This translates to double the sensitivity. The PSK (phase-shift-keying) signals have no spectral line at carrier frequency. Costas loop is a non-linear scheme which can generate such a line spectrum.

A novel architecture of NCO has been adapted to evaluate the working of the Costas loop [3]. The counter-based NCO is advantageous in reducing the quantization error by maintaining constant number of samples irrespective of the output frequency. This approach reduces the rigidity in increasing the number of possible output frequencies. It is less complex compared to CORDIC algorithm based NCO.

The paper proceeds with an outline of the BPSK demodulator scheme. The further sections concentrate mainly on the design and implementation of Costas loop, which is the heart of the demodulator. As a subsection, the design of the counter-based NCO is being discussed along with other building blocks of the Costas loop. Finally we present the simulation results of the evaluation of the Costas loop with a novel architecture of NCO adapted.

II. BPSK Demodulator

To verify the operation of a demodulator, it's necessary to generate a modulated data and hence a simple BPSK modulator. The digital implementation of BPSK modulator consists of a 2-to-1 multiplexer, an 180° phase shifter (a 2's complement block) and an NCO.

The demodulation process can be divided into two major modules – carrier recovery and clock and data recovery. The methods by which a phase-coherent carrier is derived from the incoming signal are termed, carrier recovery,and Costas-loop will be used for it. Then, the raw data is obtained by coherent multiplication, and used to derive clock-synchronization information. The raw data are then passed through the pulse shaping circuit, which shapes the pulse train so as to minimize inter-symbol-interference distortion effects. This shaped pulse train is then routed, along with the derived clock, to the data sampler which outputs the demodulated data. The implementation scheme of both the BPSK modulator and demodulator are shown in fig. 1 and 2 respectively.

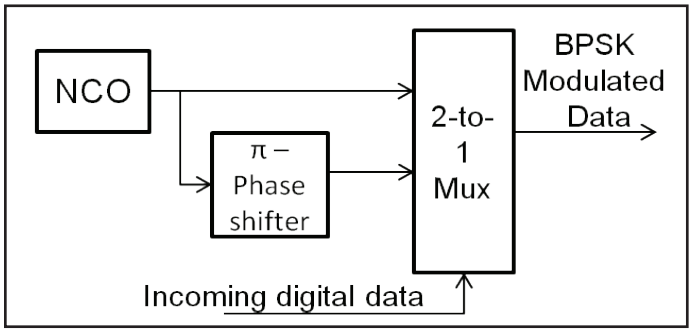

Fig. 1: Implementation Block Diagram of BPSK Modulator

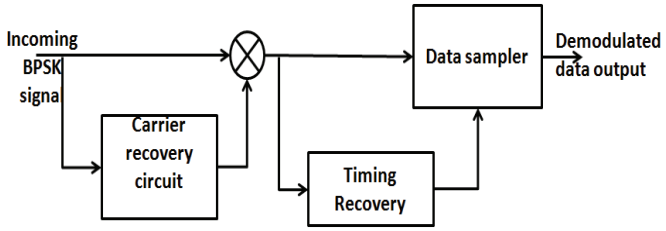

Figure. 2 Implementation Block Diagram of BPSK Demodulator

Mathematical Analysis of Costa's Loop

The mathematical model of the Costas loop is described below [4]. Let the BPSK modulated signal to the input of the Costas

loop be given by,

$$V_{in}(t) = \sqrt{2P}b(t)\cos(\omega_c t + \varphi) \quad (1)$$

Where, P – power of the carrier signal,
b(t) – modulating data,
φ – phase offset introduced by the channel.
Let the voltage controlled oscillator (with phase offset φ') output be given by,

$$V_{VCO}(t) = \cos(\omega_c t + \varphi') \quad (2)$$

where, the power content of the VCO output is assumed to be unity. The output of the I (In-phase) and Q (Quadrature-phase) arms of Costas loop is given by,

$$I = \sqrt{2P}b(t)\cos(\omega_c t + \varphi)\cdot\cos(\omega_c t + \varphi') \quad (3)$$

$$Q = \sqrt{2P}b(t)\cos(\omega_c t + \varphi)\cdot\sin(\omega_c t + \varphi') \quad (4)$$

Using trigonometry, equations (3) and (4) can be simplified to,

$$I = \frac{\sqrt{2P}}{2}b(t)[\cos(2\omega_c t + \varphi + \varphi') + \cos(\varphi - \varphi')] \quad (5)$$

$$Q = \frac{\sqrt{2P}}{2}b(t)[\cos(2\omega_c t + \varphi + \varphi') + \sin(\varphi - \varphi')] \quad (6)$$

The $2\omega_c$ t component is filtered out by the I and Q arm filters, and the DC component is proportional to (φ-φ'). Hence the outputs of I and Q are given by,

$$I_{LPF} = \frac{\sqrt{2P}}{2}b(t)\cos(\varphi - \varphi') \quad (7)$$

$$Q_{LPF} = \frac{\sqrt{2P}}{2}b(t)\sin(\varphi - \varphi') \quad (8)$$

The output of (V_m) the third multiplier is obtained by multiplying (7) and (8),

$$V_m = \frac{P}{2}b^2(t)\cos(\varphi - \varphi')\cdot\sin(\varphi - \varphi') \quad (9)$$

$$V_m = \frac{P}{4}\sin(2(\varphi - \varphi')) \quad (10)$$

since, $b^2(t) = 1$.
Thus, the Costas-loop PLL filter tracks the error signal which is proportional to sin(2(φ-φ')).

IV. Design of Costas Loop

The BPSK modulated data, with carrier frequency of 10 KHz and modulating data rate of 4 Kbps, is the input to the Costas loop. The sampling frequency of the system is set to 10 MHz. The block diagram of the Costas loop is shown in fig. 3.

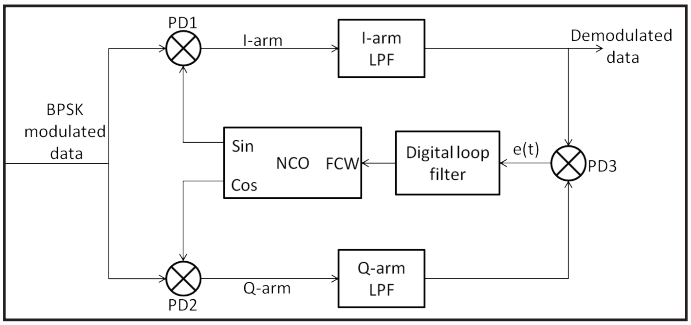

Fig. 3: Block Diagram of Costas loop

The digital implementation architecture of the Costas loop is shown in fig. 4. Fixed-point data type is used in the implementation, 16-point precision for NCO output and input, 32-point precision for filter operation. The BPSK modulated data is fed to both the phase detectors (PD's), the sine output of the NCO is fed to PD1 and cosine output to PD2. A second order Butterworth filter would do the job of the I-arm and Q-arm low pass filters. The error signal is generated by PD3 to which I-arm and Q-arm filters output fed in. The digital loop filter is implemented using integrate and dump filter, with proper gain parameters. The refined error signal from digital loop filter provides the frequency control word (FCW) for the NCO. The demodulated data, free of phase and frequency offsets, is derived out of the I-arm filter while the Q-arm filter output goes approximately zero.

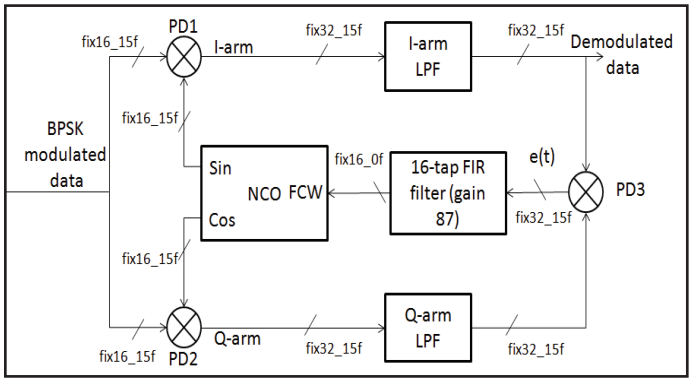

Fig. 4 Architecture of Costas Loop

A. Numerically Controlled Oscillator (NCO)

As mentioned earlier, a novel architecture of NCO is being adapted in the design of the Costas loop. The architecture of counter-based NCO is being discussed in [3] and the architecture is depicted in fig. 5. The input control word is 2-bits wide derived from the first two bits of the 16-bits wide output from the loop filter. The NCO is designed to produce the desired output frequency of 10 KHz and following are the design values:

Master clock frequency = 10MHz
Number of samples per quadrant (N) = 32
Frequency Control Word (FCW) = 1
Considering the NCO to give maximum SFDR (Spurious Free Dynamic Range), LUT word-length is chosen to $M = \log_2(4*2^N) = 7$

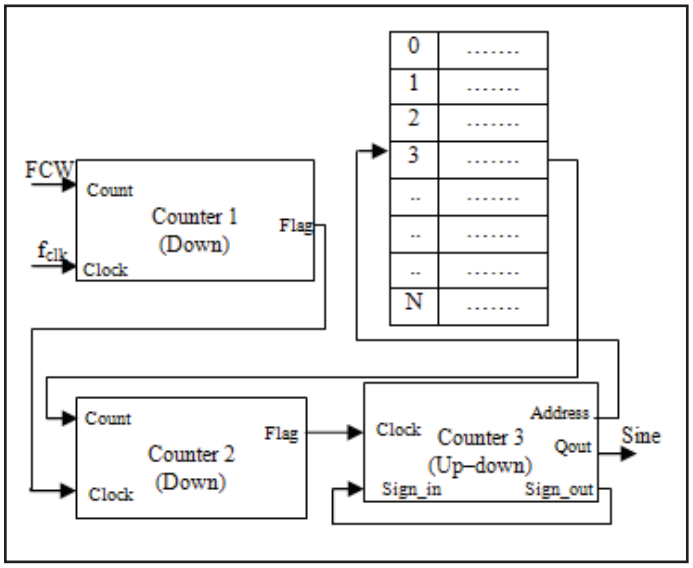

Fig. 5: Counter-based NCO Architecture

The counter-3 which is 16-bits (signed) wide and hence produces a sinusoidal whose amplitude values are 16-bits wide.

B. Low Pass Filter (LPF)

As mentioned above, a second order Butterworth low-pass filter is used for I and Q-arm LPF's. Two design parameters are to be considered: order of the filter N, cut-off frequency ω_c. The sampling frequency used is 2 MHz. The LPF has to remove $2\omega_c$ components which correspond to 20KHz and it should have bandwidth sufficient enough to allow the desired data components. Hence the cut-off frequency of the LPF is chosen to be 16KHz. The design of the filter is described below. The analog transfer function for second order Butterworth filter is given by,

$$H(s) = \frac{\Omega_c}{s^2 + \Omega_c} \quad (11)$$

where, $\Omega_c = \frac{2}{T}\tan(\frac{\omega_c T}{2})$ (12)

Then final transfer function is obtained by bilinear transformation. The filter transfer function thus obtained is,

$$H(z) = \frac{(0.00004 + 0.000078z^{-1} + 0.00004z^{-2})}{(1 - 1.9822z^{-1} + 0.9824z^{-2})} \quad (13)$$

Transposed direct form II of IIR filter is implemented, considering that direct form I structure requires more memory elements. The architecture of the LPF is shown in Figure 6.

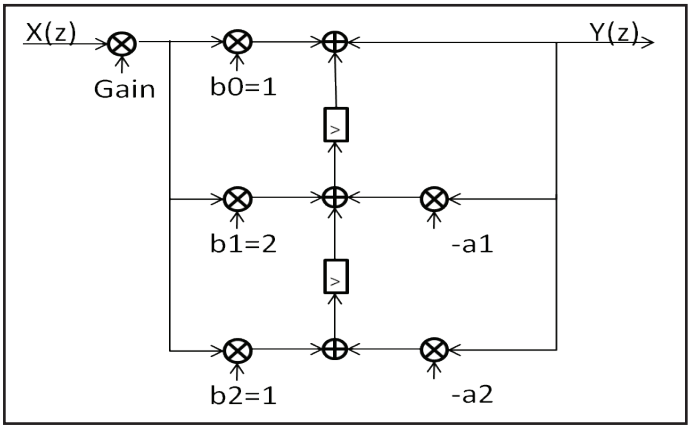

Fig. 6: Architecture of 2nd order Butterworth Filter (Transposed Direct Form-II)

C. Digital Loop Filter (FIR filter)

The purpose of loop filter is to filter the phase error signal in order to provide a better signal to the VCO. The error signal generated by the PD is actually a noisy estimate of the phase error, i.e., the error signal consists of an error term and a noise term. The loop filter processes the error signal in order to generate a useful error while suppressing the effect of the noise as much as possible.
The loop filter is essentially a low pass filter and a simple filter integrating 16 samples is used as loop filter. A 16-tap FIR filter with all coefficients set to '1' is used as loop filter. Hence the gain of the loop filter is 16.

D. Transient Analysis of the Costas Loop

The closed loop response of the Costas loop can be estimated by using the frequency domain equivalent of a PLL model. The overall loop response is controlled by the two individual low-pass filters that precede the third phase detector while the third low-pass filter serves a trivial role in terms of gain and phase margin. The NCO gain is defined as the amount by which the NCO frequency changes when the FCW changes by unity. The phase detector gain is given by the output voltage when the input frequency difference corresponds to 1Hz. An amplifier is introduced to provide desired gain to get the desired noise bandwidth.
The system transfer function of the Costas loop in the analog domain is the same as that of PLL (Fig. 7, [5]) where F(s) is given by the LPF (low-pass filter) in either I or Q-arm.
The lock range should not exceed than the loop gain [6] i.e.,

$$|\omega_{lock}| \leq K_L \quad (14)$$

where, K_L is the loop gain given by,

$K_L = K_0 K_d K_{lf} K_g$

where, $K_0 = (2\pi * 2 * 10^6)/(2^{16})$ is the NCO gain

$K_{lf} = 16$ is the loop filter gain

$K_{pd} = 1/4\pi$ is the phase detector gain

$K_g = 87$ is the additional gain

Let the lock range be $\omega_{lock} = 2\pi * 3500$radian. Since ω_{lock}, K_0, K_d, K_{lf}, are known, K_g is calculated to be around 87. This is incorporated in loop filter gain factor. Hence the final loop gain is $K_L = 21240.234$.

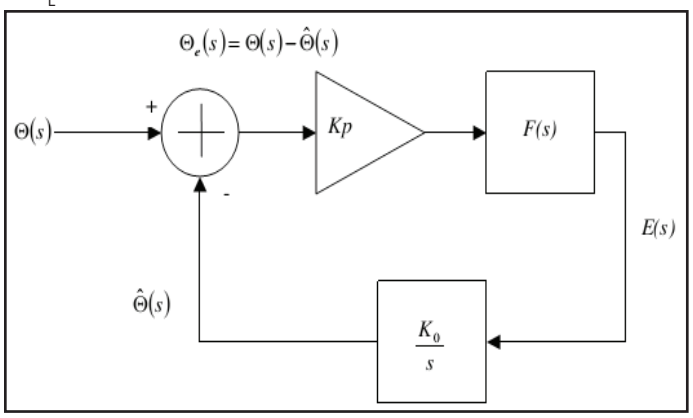

Fig. 7: Block Diagram of a Traditional PLL

V. Simulation Results and Hardware Implementation

The Costas loop is modelled using MATLAB Simulink for modulating data rate of 4Kbps and carrier frequency 10KHz. The simulation results (Fig. 8) shows that the demodulated data is same as the modulating data.

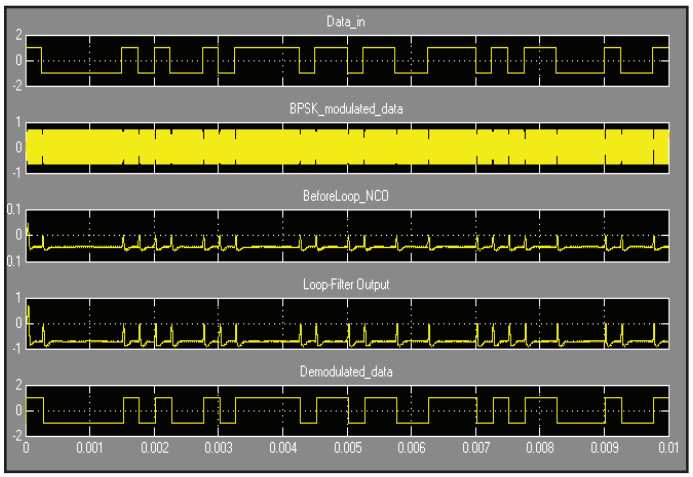

Fig. 8: Simulation output of the Costas loop Simulink model

The Costas loop design is implemented using VHDL which is then synthesized to program the FPGA. For simulation purpose, the BPSK modulator and demodulator were embedded in one

module. Internal data generator is used for simulation, which produces specific binary data of length 80 bits. Practically, the timing and phase mismatch has to be introduced in order to verify the timing and phase correcting ability of the designed BPSK demodulator. The clock variance is created by using two different local oscillators, one at transmitter and one at receiver.

The design was implemented onXC3S1500, Xilinx Spartan 3 device. The ISE Synthesis report for the design of the Costas loop is shown in fig. 9. Two different clock sources are used, one at transmitter (modulator) and one at the receiver (demodulator), to create clock variance. The BPSK modulated data, multiplier output, the output of I-arm LPF are more than one bit wide (16 and 32 bits); hence DAC is used to verify these signals. The output recorded with 10KHz subcarrier is shown in fig. 10.

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	4248	13312	31%
Number of Slice Flip Flops	794	26624	2%
Number of 4 input LUTs	8166	26624	30%
Number of bonded IOBs	6	221	2%
Number of MULT18X18s	30	32	93%
Number of GCLKs	2	8	25%

Fig. 9: Device Utilization Summary

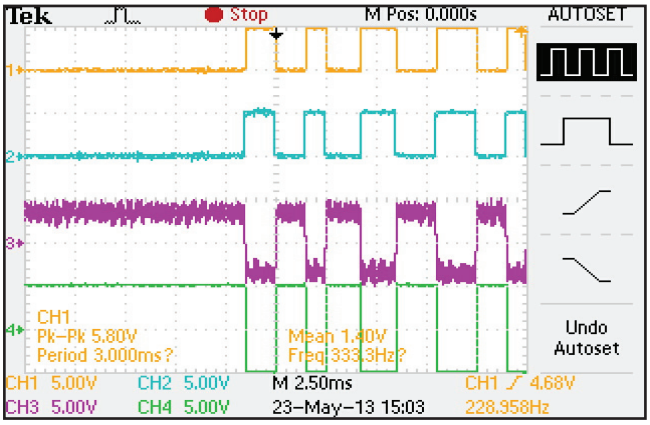

Fig. 10: BPSK Transceiver with 10KHz subcarrier, 4 Kbps data (1) Modulating data (2) Data recovered using Costas Loop (3) Multiplier (I - arm) output (4) LPF (I - arm) output

VI. Conclusion

The Costas loop is evaluated with a new scheme of NCO adapted. The Costas loop equivalent to second order PLL is capable of removing both phase and frequency offsets, with lock range up to 3.5KHz. The loop is verified for its stability by its transfer function. The design can be further modified for higher data rate and carrier frequency.

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