DSP Kit Implementation of Encoder Decoder Circuit of Reed Solomon

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Abstract

High Bit Error Rate (BER) of the communication system requires various coding methods for transferring the data. Reed-Solomon (RS) codes are very efficient for correction of burst errors in communication system. This paper describes a Reed Solomon encoder decoder implementation on the TMS320C6713 DSP. The C6713 DSK is a low-cost standalone development platform that enables users to evaluate and develop applications and provide extremely high levels of performance. Results for the encoder as well as decoder are presented.

Keywords

Reed Solomon(RS),Digital Signal Processor(DSP), Berlekamp-Massey(BM)

I. Introduction

In digital communication system, the data gets corrupted because of the lots of disturbances in the communication channel. There are many types of error correcting code schemes that are used in digital communication system for efficient transmission of data. Channel coding is the signal processing operation i.e. used for the efficient transmission of digital information over the channel. Error detection and error correction is used to reduce the level of noise and interferences [1-2]. A channel code mostly referred to the forward error correction code, wherethe sender adds redundant data to its messages. This will help receiver to detect and correct errors without the need of additional data. FEC is applied where retransmissions are relatively costly or impossible [2]. There are many types forward error correction codes but Reed-Solomon (RS) codes are very efficient in case of burst errors.

In [3] an adaptive channel RS encoding scheme is designed and Simulation of the proposed system is done on MATLAB. Relation among BER for different code rates and the performance of RS codes for various modulation schemes is analyzed.But decoder implementation is not considered. In [4] author analyzed the performance and efficiency of Reed-Solomon (RS) Codes but real time implementation using DSP is not considered [5]. Implemented the Berlekamp-Massey algorithm for decoding using DSP but do not considered the encoding part. In this paper we have focused on the real time implementation of RS encoder as well as decoder.

Rest of the paper is organized as follows. Section II describes the RS encoding as well as decoding algorithm in detail. In section III a brief introduction to the DSP kit used for the implementation is given. Section IV and V includes simulation, result and conclusion respectively.

II. RS Encoder and Decoder

RS codes are linear non binary cyclic block codes. These codes are block-based error correcting codes and are used to correct errors in many systems including storage devices,satellite communications, digital television, wireless or mobile communications,high-speed modems such as ADSL, etc.The RS encoder takes a block of digital data and adds extra "redundant" bits. Errors occur during transmission or storage because of noise, interference etc. The Reed-Solomon decoder processes each block and attempts to correct errors and recover the original data. The number of errors that corrected depends on the RS code characteristics [4, 6].

A RS code is specified as RS (n,k) with s-bit symbols. The encoder takes k data symbols of s bits each. After then it adds parity symbols to make an n symbol codeword. So there are n-k parity symbols of s bits each. RS decoder can correct up to t symbols where t = (n-k)/2. A large value of means, large number of errors corrected, but with more computational power. RS decoder can correcterrors as well aserasures.When a codeword is decoded, there are three possible outcomes. If 2s + r < 2t (s errors, r erasures) then the original transmitted code word gets recovered. But if it is not the case then the decoder either will detect that it cannot recover the original code word or will mis-decode without any indication [6].

A. Finite (Galois) Field Arithmetic

RS codes are based on Galois fields or finite fields. This field has the property that arithmetic operations on field elements always gave result that exists in the field. Such operations require special hardware or software functions for implementation [7].

B. Generator Polynomial

A RS codeword is generated using a special polynomial and the valid codewords are divisible by the generator polynomial. The generator polynomial is of the form

$$g(x) = (x - \alpha^{i})(x - \alpha^{i+1})\ldots(x - \alpha^{i+2t}) \qquad (1)$$

Message polynomial is of the form

$$m(x) = m_0 + m_1 x + \cdots + m_{k-1} x^{k-1} \qquad (2)$$

The systematic form of these codes is obtained by finding the remainder p(x) of division of $X^{n-k}.m(x) by g(x)$..

$$X^{n-k}.m(x) = q(x).g(x) + p(x) \qquad (3)$$

Code polynomial is then,

$$c(x) = X^{n-k}.m(x) + p(x) \qquad (4)$$

The code word is transmitted and received at the receiver. This codeword is now entered to RS decoder for decoding. the decoder first tries to check if this codeword is a valid codeword or not. If it does not, errors occurred during transmission. There are two main parts in RS decoder, error detection part and error correction part respectively.

C. Error Detection "Syndrome Calculation"

The first step is to check if there exists any error in the codeword or not and is done using syndrome computation block.Let the transmitted codeword polynomial, received codeword polynomial and error polynomial formed as follow[5]:

$$c(x) = c_0 + c_1 X + \ldots\ldots + c_{n-1} X^{n-1}, \;\; where \;\; c_i \in GF(2^m) \qquad (5)$$

$$r(x) = r_0 + r_1 X + \ldots\ldots + r_{n-1} X^{n-1}, \;\; where \;\; r_i \in GF(2^m) \qquad (6)$$

$$e(x) = e_0 + e_1 X + \ldots\ldots + e_{n-1} X^{n-1}, \;\; where \;\; e_i \in GF(2^m) \qquad (7)$$

Error polynomial e(X) is related to the received polynomial r(X) and the transmitted polynomial c(X) as follows:

r(X) = c(X) + e(X) (8)

As discussed earlier the transmitted polynomial c(x)should be multiple of the generator polynomial g(X), so the roots of g(X) should give zero in the received polynomial if the error polynomial is zero. i.e., no errors occurred.Let the syndrome polynomial S(x) formed as:

$$S(x)=\sum_{i=1}^{2t} S_i x^{i-1} \qquad (9)$$

where, $i=1,2,................,2t$.
and coefficient are as follows:

$$S_i = r(\alpha^i), i=1,2,.........,2t$$

For no error, all syndrome coefficients should give zero. there is an occurrence for error occurred if there is any non-zero coefficient. [6]

D. Error Correction

The main function of the decoding algorithm used for error correction and data recovering is to get the error location polynomial σ(x), and the error evaluator polynomial W(x), which represents the locations and the values of the errors respectively. There exists two categories of decoding algorithm

1. Serial algorithms is the one in which the error locator polynomial σ(x) is calculated first and then substituted in the key equation to calculate the error evaluator polynomial W(x), e.g. (Berlekamp–Massey algorithm).
2. Parallel algorithms is the one in which the error locator polynomial σ(x) and the error evaluator polynomial W(x) are calculated in parallel, e.g. (Euclidean algorithm).[5]

In this paper we have used Berlekamp-Massey Algorithm

E. Berlekamp-Massey Algorithm

The Berlekamp–Massey (B-M) algorithm is a method i.e. used for the decoding of RS and BCH codes. Let the error polynomial e(X) contains τ errors placed at positions $X^{j1}, X^{j2},..........., X^{j\tau}$ with error values $e_{j1}, e_{j2},............, e_{j\tau}$ then:

$$e(X)=e_{j1}X^{j1}+e_{j2}X^{j2}+.......+e_{j\tau}X^{j\tau} \qquad (10)$$

Now we have to calculate the values of e_{ji} and the powers of X^{ji}.
We have 2t syndrome coefficients. Each syndrome coefficient S_i can be expressed as:

$$s_i = r(\alpha^i) = c(\alpha^i) + e(\alpha^i) = e(\alpha^i) \qquad (11)$$

From both above equations, we can obtain set of equation that relates the error locations and values to the syndrome coefficient in the form of:

This set of equation can be simplified in the form:

$$s_1 = r(\alpha) = e(\alpha) = e_{j1}\alpha^{j1} + e_{j2}\alpha^{j2} + ...+ e_{j\tau}\alpha^{j\tau}$$
$$s_2 = r(\alpha^2) = e(\alpha^2) = e_{j1}\alpha^{2j1} + e_{j2}\alpha^{2j2} + ...+ e_{j\tau}\alpha^{2j\tau}$$

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$$s_{2t} = r(\alpha^{2t}) = e(\alpha^{2t}) = e_{j1}\alpha^{2tj1} + e_{j2}\alpha^{2tj2} + ...+ e_{j\tau}\alpha^{2tj\tau}$$

$$s_1 = r(\alpha) = e(\alpha) = e_{j1}\beta_1 + e_{j2}\beta_2 + ...+ e_{j\tau}\beta_\tau$$
$$s_2 = r(\alpha^2) = e(\alpha^2) = e_{j1}\beta_1^2 + e_{j2}\beta_2^2 + ...+ e_{j\tau}\beta_\tau^2$$

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$$s_{2t} = r(\alpha^{2t}) = e(\alpha^{2t}) = e_{j1}\beta_1^{2t} + e_{j2}\beta_2^{2t} + ...+ e_{j\tau}$$

$$where,\ \beta_i = \alpha^{ji}\ and\ i=1,2,3,.....,\tau$$

From above equation, we have 2t equations in 2t unknowns as worst case, but these equations are not linear equations so we define the two polynomials i.e. the error locator polynomial σ(x) and error evaluator polynomial W(x) which presents the values of the errors.BM algorithm is a serial algorithm so firstly it will calculate location polynomial σ(x) followed by the error evaluator polynomial W(x).

III. DSP Kitarchitecture

The 6713 DSK is a standalone development platform that enables consumer to evaluate and develop applications for the TI C67XX DSP series family. It is a hardware reference design for the TMS320C6713 DSP. This DSK have The 6713 DSK is a low-cost standalone development platform that enables customers to evaluate and develop applications for the TI C67XX DSP family Flash is attached to CE1 of the EMIF in 8-bit mode. 3.5mm audio jacks are available that correspond to microphone input are used for the analog audio I/O is done through. CPLD which is a programmable logic deviceis used to implement glue logic that ties the board components together. CPLD in the kit has a register based user interface that lets the user configure the board by reading and writing to the CPLD registers. The registers reside at the midpoint of CE1 [8].

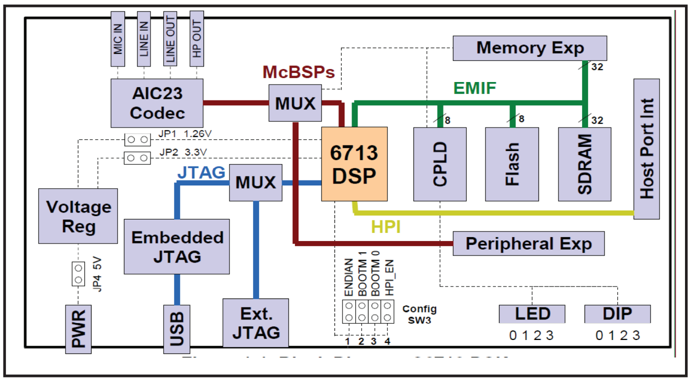

Fig. 1: DSP kit C6713 Architecture

It includes 4 LEDs and 4 DIP switches for user interactive feedback. To power the board 5V external power supply is used. On-board voltage regulators are used to provide the 1.26V DSP core voltage, 3.3V digital and 3.3V analog voltages. Communication with the DSK is done through an embedded JTAG emulator with a USB host interface. Key features include:

- Operating frequency 225 MHz
- 16 Mbytes of synchronous DRAM
- 4 user accessible LEDs and DIP switches
- 512 Kbytes of non-volatile Flash memory (256 Kbytes usable in default configuration)
- Configurable boot options
- Software board configuration through registers implemented in CPLD
- Single voltage power supply (+5V)
- Standard expansion connectors for daughter card use
- JTAG emulation [8]

VI. Result

The encoder and decoder circuit of Reed Solomon code (15, 9) is successfully implemented on DSP kit. For decoding we have usedBerlekamp-Massey algorithm. The code for encoding and decoding was written in c language. The result has been obtained after running the program on DSP kit is given below:

Look-up tables for GF (2** 4)

i	alpha_to[i]	index_of[i]
0	1	-1
1	2	0
2	4	1
3	8	4
4	3	2
5	6	8
6	12	5
7	11	10
8	5	3
9	10	14
10	7	9
11	14	7
12	15	6
13	13	13
14	9	11
15	10	12

After receiving the code word it aws decoded successfully as shown in the table given below with 100% accuracy

Results for Reed-Solomon code (n= 15, k= 9, t= 3)

i	data[i]	recd[i](decoded)
0	15	15
1	13	13
2	10	10
3	0	0
4	6	6
5	13	13
6	8	8
7	6	6
8	8	8
9	1	1
10	2	2
11	4	4
12	15	15
13	9	9
14	3	9

V. Conclusion

In this paper we have implemented the encoding and decoding circuit of Reed Solomon code successfully on DSP kit TMS32C677XX. The RS (15, 9) is developed in this. Systematic encoder is used for encoding and the Berlekamp-Massey Algorithm for decoding. The advantage of this algorithm is that there is no need to calculate the error values, as it is enough to determine the position of the errors to perform the error correction. This algorithm is works in iterative manner, so it is quite complex. We can work on Euclidean Decoder in future to remove the iterative complexity and can compare their performance.

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