

Comparative Analysis of Pulsed Latch and Flip-Flop based Shift Registers for High-Performance and Low-Power Systems

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Abstract

An optimized area-efficient shift register is proposed using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A 64-bit shift register using pulsed latches was implemented by using an 180nm CMOS process with VDD = 1.8V at the clock frequency of 100MHz.

Keywords

Flip-Flop, Pulsed Latch, CMOS Process, Non-Overlap

I. Introduction

Low power circuit design has emerged as a principal theme in today's electronics industry. In the past, major concerns among researchers and designers for designing integrated circuits were on area, speed, and cost; while secondary importance was paid to power dissipation. In recent years, however, this scenario has changed and now developing of different circuit techniques for low power circuit design is an important research area. On designing any combinational or sequential circuits, the power consumption, implementation area, speed, voltage leakage, and efficiency of the circuit are the important parameters to be considered initially. These parameters are inter related to each other so in order to obtain few parameters remain may have less preference. Shift register have several type of applications like data conversion between parallel to serial or serial to parallel, counters, parity generator, etc. Coming to the real time applications like image processing ICs [4]-[6], digital filters [1] and communication receivers [3] also we are using shift registers. Let consider the shift register application in image processing. As the size of the image data continues to increase due to the high demand for High quality image data, the word length of the shifter register increases to process large image data in image processing ICs [3]. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. Our proposed project is to reduce the power and area of the circuit by replacing the flip-flops with the latches in the shift register.

This paper is organized as follows. Section II provides an overview of the various types of Flip-Flops in terms of their advantages and drawbacks, and section III describes the analysis of proposed pulsed latch based shift register. Section IV provides schematics of Flip-Flop and Pulsed Latch based shift registers of various sizes and clock pulse generator which are drawn in S-Edit. Simulation results from HSPICE using 180nm PTM technology with VDD=1.8V and their comparisons are presented in Section V and conclusion is drawn in Section VI.

II. Conventional Methods

In conventional method shift register is designed by serial connection of the master-slave flip flops. The following figure shows the master slave flip flop.

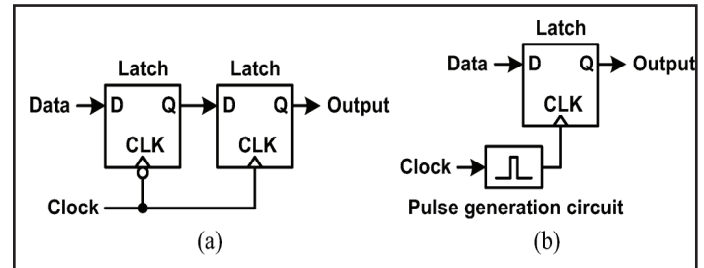


Fig. 1: Master Slave Flip Flop

The PowerPC master-slave latch (Fig. 1), presented in [2], is one of the fastest classical structures. Its main advantages are a short direct path and low-power feedback. But one has to keep in mind another aspect of this structure is its large clock load [7], which greatly influences the total power consumption on-chip.

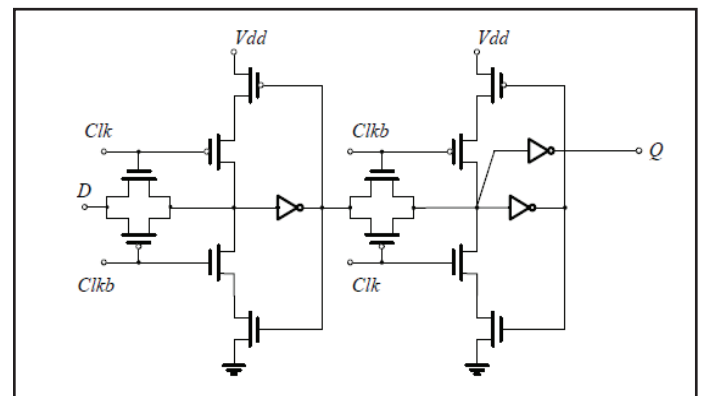


Fig. 2: PPCFF

Hybrid-latch flip-flop (HLFF) (Fig. 3), presented in [10], and is one of the fastest structures presented. It also has a very small PDP. The major advantage of this structure is its soft-edge property, i.e., its robustness to clock skew. One of the major drawbacks of the hybrid design in general is the positive hold time, discussed in Section II-B. Due to the single-output design, the power-consumption range of the HLFF is comparable to that of the static circuits. However, depending on the power distribution, pre charged structures can dissipate more than static structures for data patterns with more "ones". Hybrid design appears to be very suitable for high-performance systems with little or no penalty in power when compared to classical static structures [7].

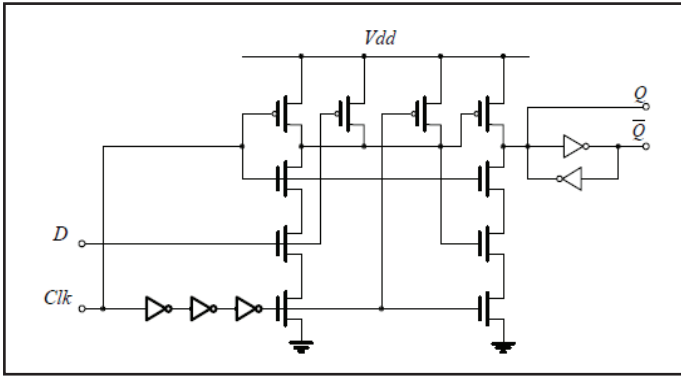


Fig. 3: HLFF

Another interesting approach to hybrid design is the semi-dynamic flip-flop (SDFF) structure (Fig. 4) presented in [16]. It is the fastest of all the presented structures. The significant advantage over HLFF [9] is that there is very little performance penalty for embedded logic functions. The disadvantages are bigger clock load and larger effective pre charge capacitance, which results in increased power consumption for data patterns with more “ones.” This is still the most convenient structure or applications where speed is of primary importance, without a big penalty in power consumption.

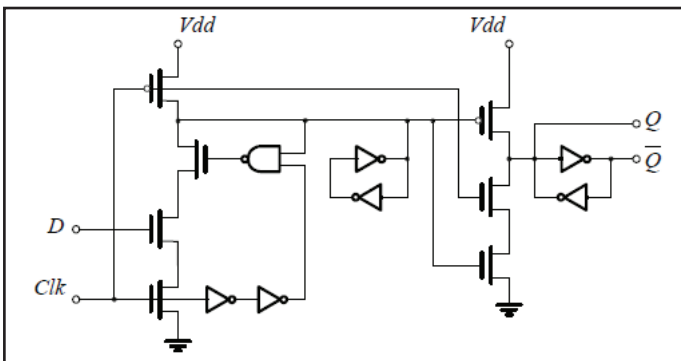


Fig. 4: SDFF

Optimized shift register designs are not achieved with the use of master-slave flip flops. Performance parameters such as area and power can be reduced with use of pulsed latches. Hence master-slave using two latches can be replaced by pulsed latch consisting of latch with pulsed clock signal [7] which is shown in fig. 5.

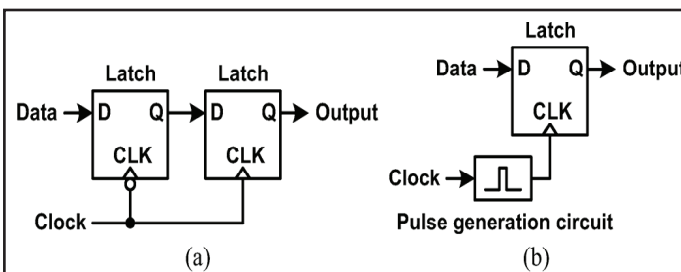


Fig. 5: Pulsed Latch

III. Proposed Shift Register

Proposed work is a low-power and area-efficient shift register using pulsed latches. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional

temporary storage latches. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop.

The pulsed latch cannot be used in shift registers due to the timing problem occurred in latch. The following figures show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the inputs signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width.

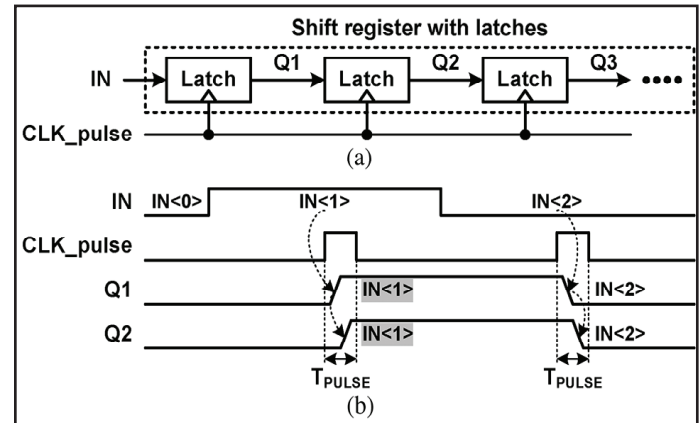


Fig. 6(a): Series Connection of Latches (Shift Register) (b) Timing Problem in Latches.

This timing problem can be overcome with the use of multiple non overlapped delayed pulsed clock signals. The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data.

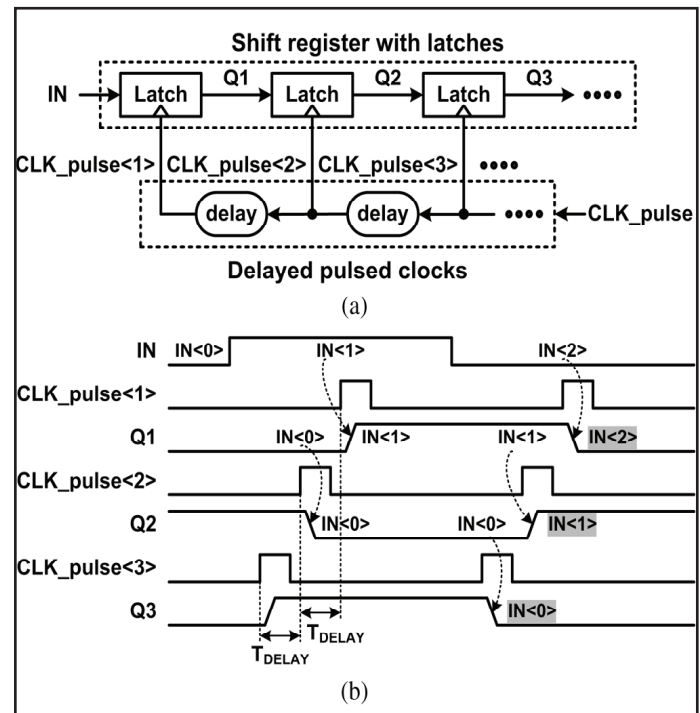


Fig. 7: Shift Register With Latches and Delayed Pulsed Clock Signals. (a) Schematic. (b) Waveforms.

Below figure shows an example the proposed shift register. The proposed shift register is divided into M sub shifter registers

to reduce the number of delayed pulsed clock signals. A 4-bit sub shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals (CLK_pulse<1:4> and CLK_pulse<T>). In the 4-bit sub shift register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Five non-overlap delayed pulsed clock signals are generated by the delayed pulsed clock generator. The operations of the other sub shift registers are the same as that of the sub shift register #1 except that the first latch receives data from the temporary storage latch in the previous sub shift register.

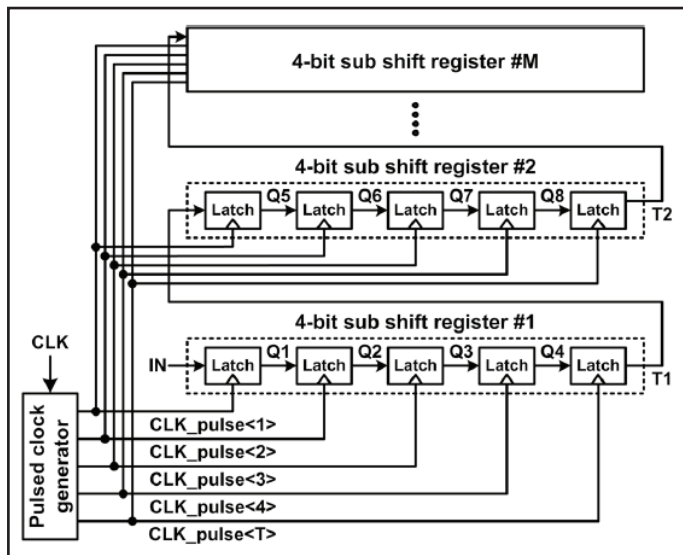


Fig. 8: Proposed Shift Register

When an N-bit shift register is divided into K-bit sub shift registers, the number of clock-pulse circuits is K+1 and the number of latches is N+N/K. A K-bit sub shift register consisting of K+1 latches requires K+1 pulsed clock signals. The number of sub shift registers M becomes N/K, each sub shift register has a temporary storage latch. Therefore, N/K latches are added for the temporary storage latches. A 64-bit shift register with sub shift register size 4 (K=4) requires 16 sub shift registers. And each sub shift register consist of 5 latches.

Below figure is the pulse clock generator. Which gives the multiple non overlap delayed pulse clock signals for K-bit sub shift register.

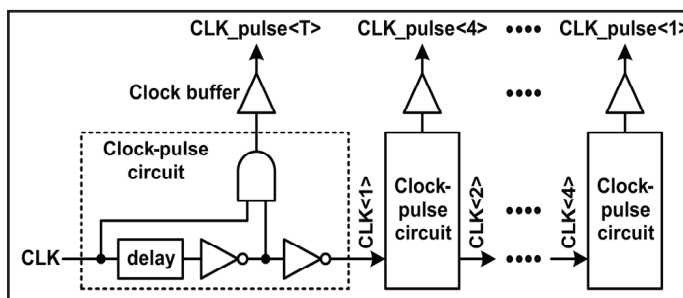


Fig. 9: Non Overlap Clock Pulse Generator

SSASPL (static differential sense amp shared pulse latch) is a smallest all pulsed latches [7]-[10]. The schematic of SSASPL is shown in below figure.

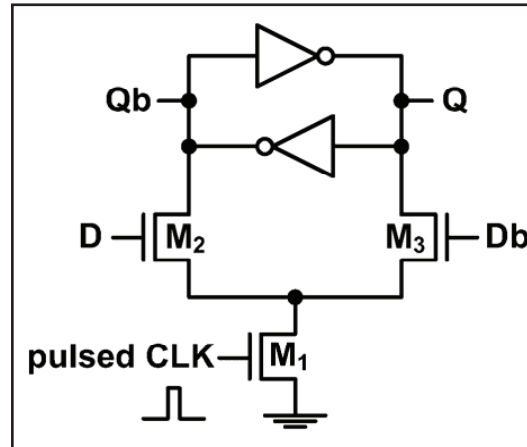


Fig. 10: Schematic of SSASPL [7]

PPCFF (power pc style flip flop) is a smallest flip flop [11]-[15] with the total number of transistors as 18. So in this paper we are compared the performance of shift register by using flip flop and pulsed latch that is PPCFF and SSASPL respectively.

IV. Schematics and Simulation Results

A. Schematics of Shift Registers

All the shift registers schematics are drawn in S-Edit of Tanner Tools and from which net lists are extracted, which are given as input files for the H-Spice. Simulations are carried out in H-Spice and wave forms are generated using Avan waves.

When counting the total number of transistors in pulsed latches and flip-flops, the transistors for generating the differential clock signals and pulsed clock signals are not included because they are shared in all latches and flip-flops. The SSASPL uses 7 transistors, which is the smallest number of transistors among the pulsed latches [7]-[9]. The PPCFF uses 16 transistors, which is the smallest number of transistors among the flip-flops [11]-[15]. Two 64-bit area-efficient shift registers using the SSASPL and PPCFF were implemented to show the effectiveness of the proposed shift register. Fig. 11 shows the schematic of the PPCFF, which is a typical master-slave flip-flop composed of two latches. The PPCFF consists of 16 transistors and has 8 transistors driven by clock signals. For a fair comparison, it uses the minimum size of transistors.

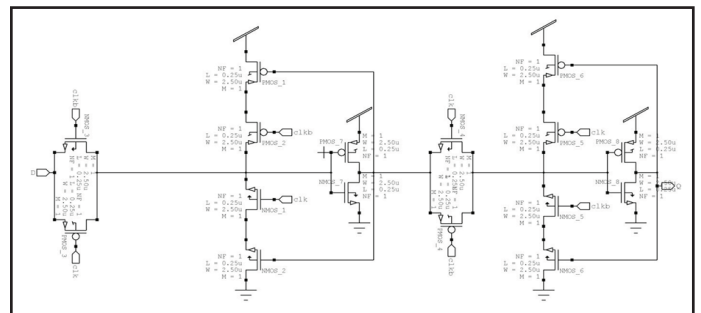


Fig. 11: Schematic of PPCFF

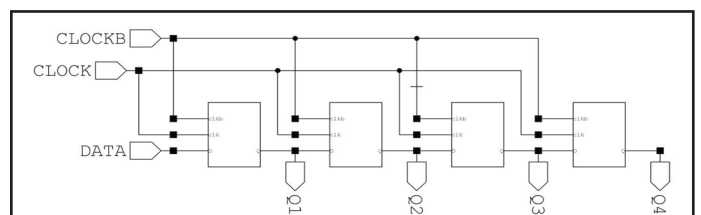


Fig. 12: 4-bit Shift Register Using PPCFF

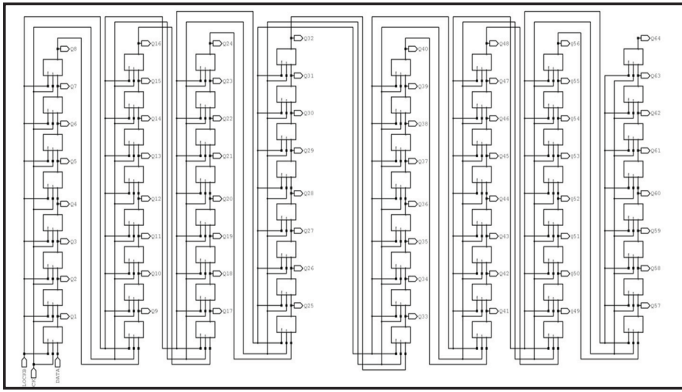


Fig. 13: 64-bit Shift Register Using PPCFF

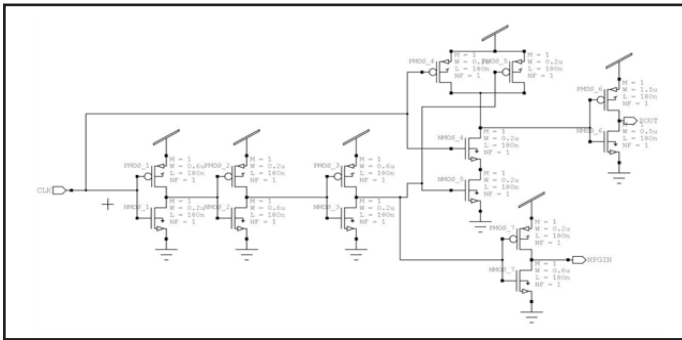


Fig. 14: Pulse Generation Circuit

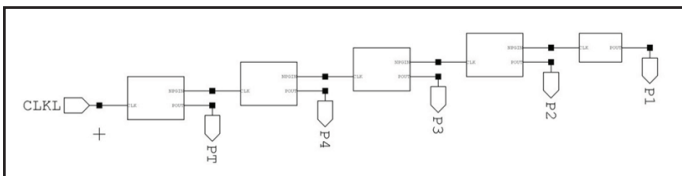


Fig. 15: Five Non-Overlapped Clock Pulses Generator

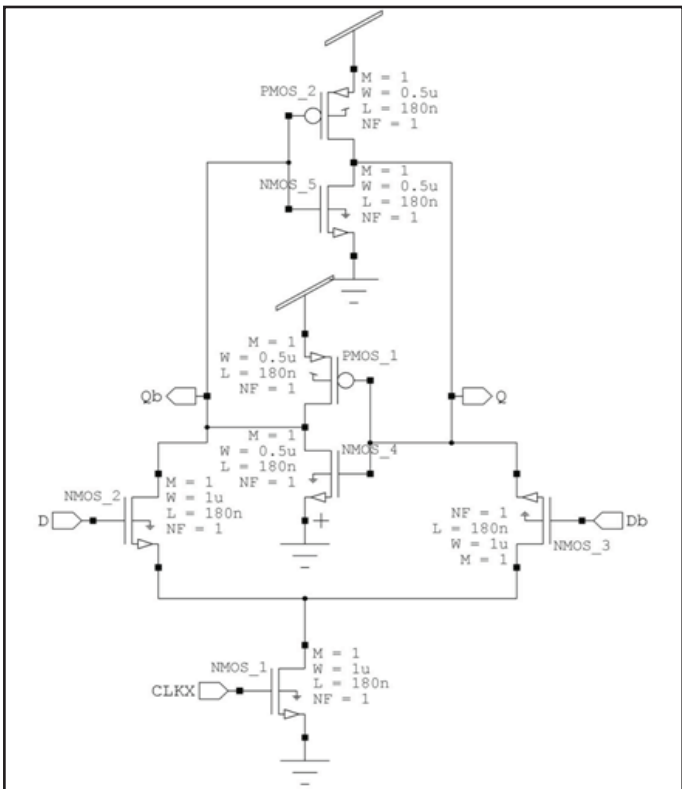


Fig. 16: Schematic of SSASPL latch

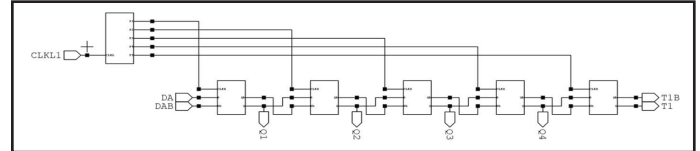


Fig. 17: 4-bit Shift Register Using SSASPL

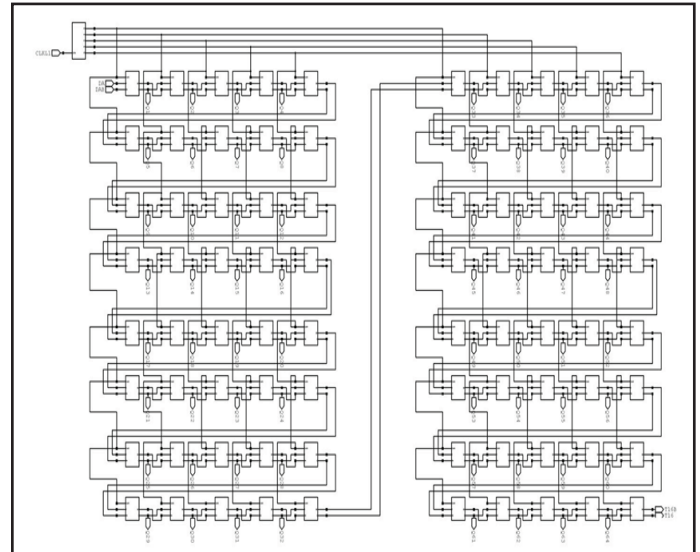


Fig. 18: 64 Bit Shift Register Using SSASPL

B. Simulated Waveforms

To compare the performances of the proposed shift register with the flip-flop based shift register, each circuit was designed using 180nm technology with VDD=1.8V, fCLK=100MHz, Temp=250C and simulated with HSPICE. The waveforms for the three comparators are shown below.

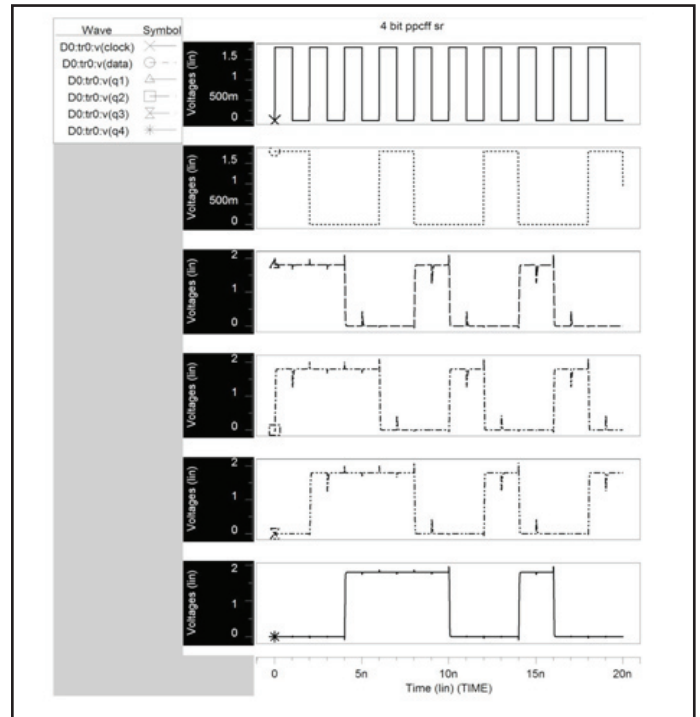


Fig. 19: Simulated Wave Forms for PPCFF 4-Bit Shift Register

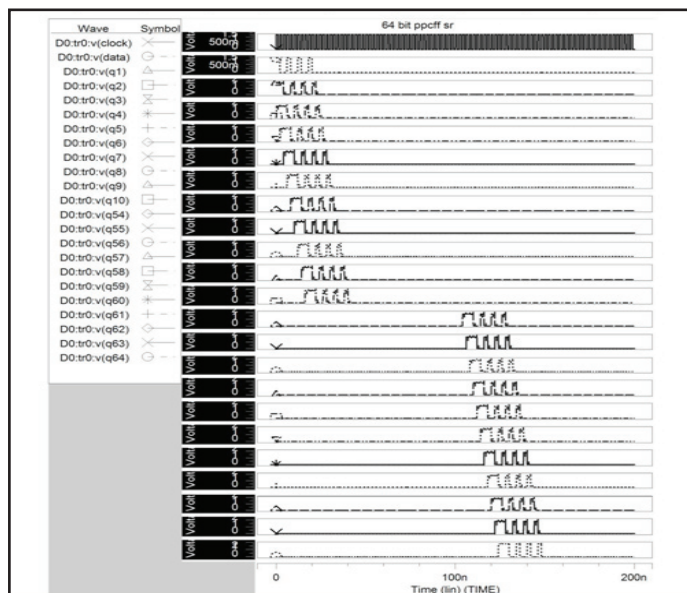


Fig. 20: Simulated Wave Forms for PPCFF 64-Bit Shift Register

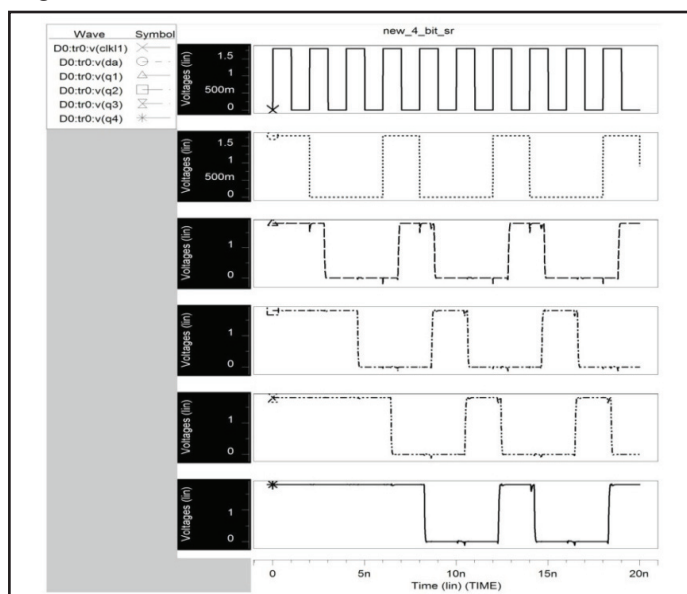


Fig. 21. Simulated waveforms for SSASPL four bit shift register

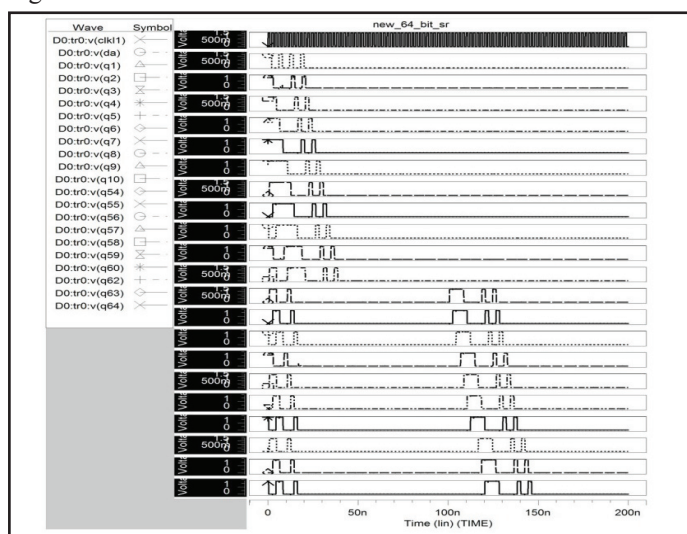


Fig. 22. Simulated wave forms for SSASPL 64-bit shift register

V. PERFORMANCE COMPARISON

Table 1 shows the performance comparisons of shift registers. The conventional shift register using flip-flops was implemented with the PPCFFs. The proposed shift register using pulsed latches were implemented with the SSASPLs. The proposed shift register achieves a small area and low power consumption compared to the conventional shift register as the numbers of transistors are less.

Table 1:

Size of SR	Shift Register using SSAPL (Pulsed Latch)		Shift Register using PPCFF (Flip-Flop)	
	Total No. of transistors	Power (mW)	Total No. of transistors	Power (mW)
4-BIT	103	0.227	64	0.140
8-BIT	138	0.241	128	0.224
16-BIT	208	0.274	256	0.343
32-BIT	348	0.311	512	0.373
64-BIT	628	0.313	1024	0.422

VI. Conclusion

The shift register reduces area and power consumption by replacing flip-flops with pulsed latches. A 64-bit shift register was implemented using a 0.18 μm CMOS technology with $v_{dd}=1.8\text{V}$ at clock frequency of 100 MHz. which consumed the power and area compared to conventional method that is shift register using flip flops.

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