Design and Analysis of Comparators using 180nm CMOS Technology

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Abstract
The real world signals are mostly analog in nature and hence, an analog to digital converter is needed to transmit effectively the analog signals to digital signals. This paper describes the comparator circuits used in most of the analog circuits now-a-days. Comparators play a vital role in most of the analog circuits like Flash ADC's and the performance of these circuits is greatly influenced by the choice of comparators. In this paper, first a " Open loop comparator" is designed and its analysis is done followed by a "TIQ comparator", "Quantized Differential Comparator", "Two stage CMOS amplifier with an output inverter" and "CMOS-LTE Comparator" and all of these circuits are used for implementing a lot low power analog circuits. After implementing all the comparator circuits, power and delay analysis has been done on the basis of which Power-Delay-Product (PDP) has been calculated. All the above circuits are implemented using 180nm CMOS technology using a supply voltage of 1.8v. TANNER EDA environment is used for design and simulation of these circuits.

Keywords
CMOS comparator, TIQ comparator, low power, differential comparator, CMOS-LTE, Tanner EDA.

I. Introduction

The comparator is a circuit which compares one analog signal with another analog signal or a reference signal and produces binary signal as the output based on the comparison. Comparators are also known as 1-bit analog-to-digital converter. Fig. 1 shows symbol of comparator.

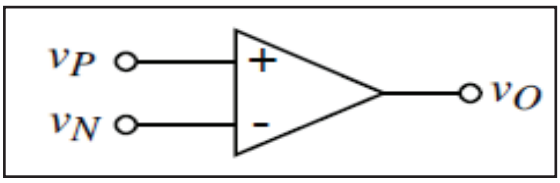


Fig. 1: Symbol of a Comparator

In Analog-to-Digital converters (ADC), comparators play an important role. The performance of the target application is significantly influenced by the type and architecture of the comparator. The comparators, the delay, input offset voltage and input signal range directly affects the speed and resolution of an ADC. Some fundamental applications of comparators are analog-to-digital conversion, signal detection, neural networks and function generation etc.

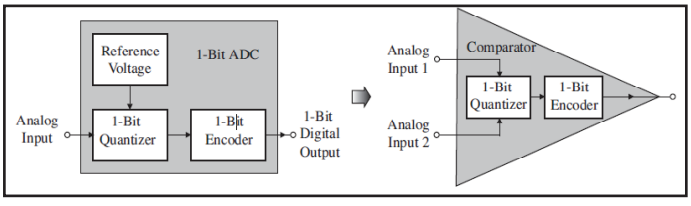


Fig. 2: The Block Diagram of a Comparator

This paper is organized into six sections. Section 1explaines all about comparators in general. Section II discusses the design of a "Two stage open loop comparator using 180nm Cmos technology". Section III discusses "TIQ Comparator" and its disadvantages. Section IV gives the Quantized differential Comparator followed by the explanation of two stage CMOS amplifier with an output inverter section V. Section VI deals with CMOS-LTE Comparator and Section VII deals with implementation and results of the above circuits using CMOS technology in TANNER EDA environment.

II. Two Stage Open Loop Comparator

Two stage open loop comparator circuits consist of two differential inputs. This comparator consists ofdifferential amplifier, input stage, and output stage as shown in Fig. 3. One of the advantages of this circuit is that the circuit consumes minimum number of transistor and thus the circuit area is small.

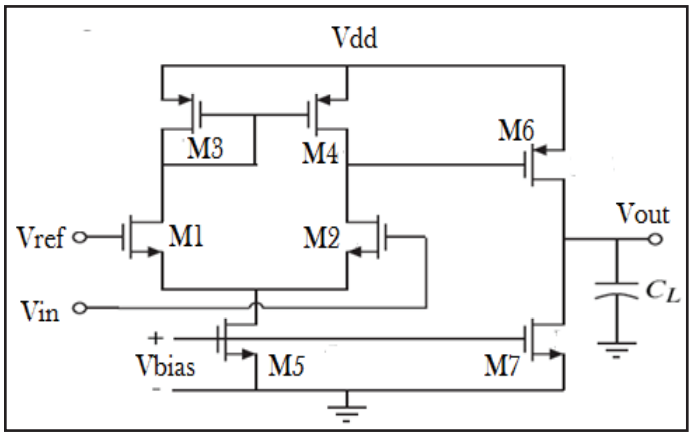


Fig. 3: Two Stage Open Loop Comparator

In order to implement a high gain, open-loop comparator, the two-stage op-amp without compensation will be an excellent implementation. In order to achieve the desired resolution Comparator requires differential input and sufficient gain. So, two stage op-amps make an excellent implementation of the comparator. Hence a simplification occurs because it is not necessary to compensate the comparator as it will generally be used in an open loop mode. In fact, the comparator has the largest bandwidth possible if it is not compensated and hence the large bandwidth gives a faster response.

The two stage open loop comparator can be designed by using the following formulas:

$(W6/L6) = (2I6)/ (Kp'*(VSD6\ (sat))^2)$; (i)
$(W7/L7) = (2I7)/ (KN'*(VDS7\ (sat))^2)$; (ii)
$(W3/L3) = (W4/L4) = (I5)/ (Kp'*(VSG3-|VTP|)^2)$; (iii)
$(W1/L1) = (W2/L2) = gm12/(KN*I5)$; (iv)
$(W5/L5) = (2I5)/(KN'*(VDS5(sat))^2)$; (v)
Where, $I6=I7= (|Pll|*Cll)/(\lambda n + \lambda p)$; (vi)
$|Pll| = 1/(tp*(mk)\ 1/2)$; (vii)
$I5= (2*I7*Cl)/Cll$; (viii)

III. TIQ (Threshold Inverter Quantization) COMPARATOR

The technique's name is so due to the use of two cascading inverters as a voltage comparator. The voltage comparators compare theinternal reference voltages with input voltage, which are determined by the transistor sizes of the inverters. Hence, the resistor ladder circuit used is not required as in a conventional flash ADC. The Comparator's role is to convert an input voltage (VIN) into logic `1' or `0' by comparing a reference voltage (Vref) with the VIN. If VINis greater than Vref, the comparator produces an output which is `1', otherwise `0'. The TIQ comparator uses two cascading CMOS inverters as a comparator for low power consumption and high speed as shown in fig. 4.

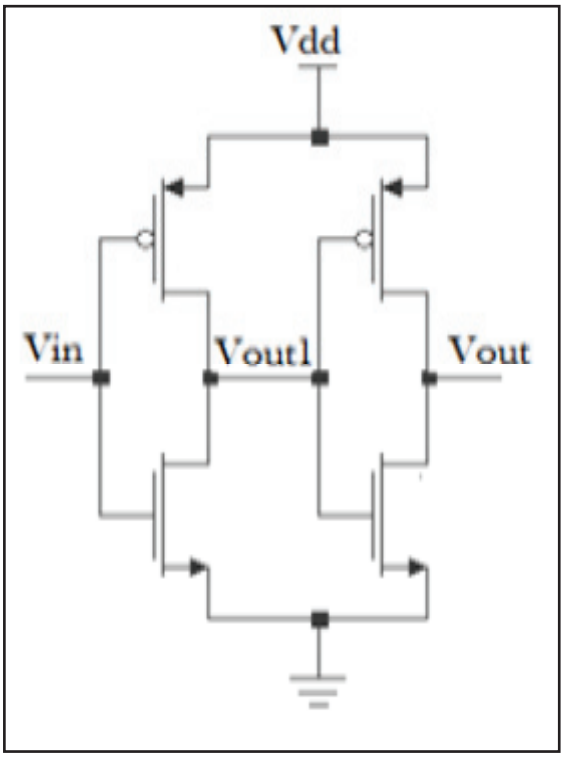


Fig. 4: TIQ Comparator

The use of second inverter is to increase voltage gain and to prevent an unbalanced propagation delay. Keeping the length of the PMOS and NMOS devices fixed, we can get desired values by changing only the width of the PMOS and NMOS transistors. We take the assumption that both transistors are in the active region, the gate oxide thickness (Cox) for both transistors are same, and the lengths (Lp and Ln) of both transistors are also the same. So, Vm is shifted depending upon the transistor width ratio (Wp/Wn). Hence, increasing Wp makes Vm larger and increasing Wn results in Vm being smaller on the VTC.

However, in order to use the CMOS inverter which acts as a voltage comparator, we should check the sensitivity of Vm to other parameters, which are not taken into consideration, for correct operation of the TIQ comparator. In a mixed-signal design, the ignored parameters like threshold voltages of both transistors, electron and hole mobility, and power supply voltage are not fixed at a constant value.

There are some distinct disadvantages of the TIQ approach:

1. The structure is single-ended.
2. Due to poor power supply rejection ratioit requires a separate reference power supply voltage for analog part only.
3. Due to process parameter variations,it has slight changes in linearity measures (DNL, INL) and the maximum analog input signal range. However, these problems can easily be handled by front end signal conditioning circuitry.
4. In order to reduce the power consumption and increase the performance during metastable stage it requires an S/H at the analog input.

IV. Quantized Differential Comparator

Quantized Differential Comparator technique is basically used for low voltage applications of Flash ADC's. The internal reference voltages, which are calculated by the transistor sizes of the Quantized Differential Comparator, are then compared with the input voltage. The comparator produces an output '1' or '0' depending on applied input voltage. If we take the case of conventional differential comparator, the transistor sizes are matched and the input Vb is taken from Reference Voltage (Vref) generated by resistor ladder circuit. Thus all the comparators of n-bit flash ADC are identical. On the other hand, to create an offset voltage in Quantized Differential Comparator, we use different transistor sizes of the transistor M2 of the differential pair. And also, input voltage is applied to the V1 terminal and the voltages at V2 and Vb are constants (Figure 5). With this intentional mismatch in the differential pair,the desired internal reference voltage is generated. On this basis, 2n-1different sizes of comparators are needed for the flash ADC implementation. The inverter is used at the output of the differential amplifier to get sharp Voltage Transfer Characteristic (VTC) curves.

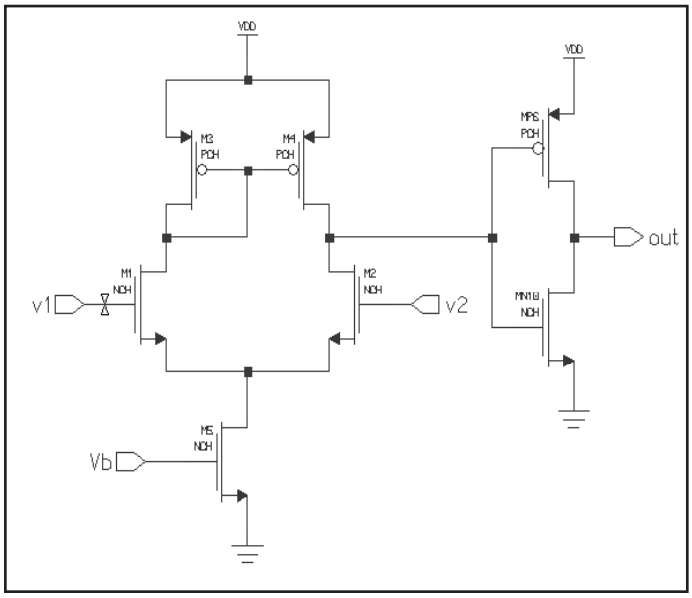


Fig. 5: Quantized Differential Comparator

In order to design n-bit flash ADC, one needs 2n-1 equal quantization voltages, and those many numberof Quantized Differential Comparators. In order to generate the different sizes of transistors for different reference voltages of the comparators, a PERL code has been developed and the device sizes have been picked up from the data generated to match the requirements. Once the comparators produce a thermometer code, the thermometer decoder is used, which generates 1-out-of-n code, using XOR logic.

V. Two Stage CMOS Amplifier with an Output Inverter

This comparator circuit is a two–stage CMOS amplifier with an output inverter consisting a total of three stages. The first is a differential pair, the second stage is a common source amplifier and is an inverting buffer. The input bias current is designed for 1µA in this circuit. The total amount of bias current is 3µA, as the

current is mirrored to the first two gain stages. Both the analog inputs are connected to the differential pair. The refernce voltage is set as 'Vim' in this circuit. The transistors length is chosen to be 180nm as speed is more important than gain in this circuit design. Since NMOS transistors have higher mobility than PMOS transistors, an NMOS differential pair is used.

In order to improve gain of the first stage and lower the input offset voltage , the widths of the input differential pair NMOS1-NMOS2 were increased to get better matching. A commomsource amplifier is usec to get overall agin of the amplifier.The area covered by the common source transistorPMOS2 is increasedwith the goal of reducing the high parasitic capacitance ofPMOS2 which causes delay in the first stage. This causes decrease in the propagation delay of the circuit. The thirdstage is an inverter buffer which increases slew rate of the circuit and adds modest gain. The circuit designed in fig. 6 gives the length, width and multiplier values for each transistor.

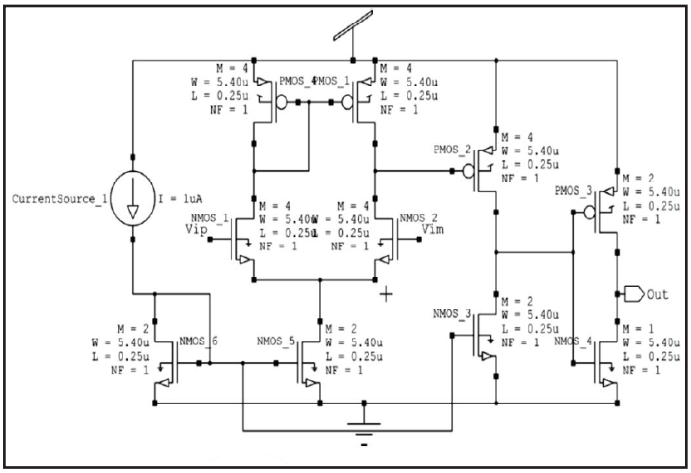


Fig. 6: Two Stage CMOS Amplifier With an Output Inverter Comparator

VI. CMOS-LTE Comparator

CMOS inverter is the well-knownsimplest voltage-to-current transducer (VCT) implemented in CMOS technology. The inverter has very low distortionand very good frequency response,as shown by experiment and simulation howeverthe linear behavior depends severely on the matching between p-channel and the n-channel transistors; i.e., the parameter μμeffCoxW/L must be the same for both the transistors and its power supply rejection (PSR) is also poor. The MOS parameters in the above expression have their usual meaning. Perfect matching is difficult to achieve in practice because the effective mobilities μeffof electrons and holes depend on doping, bias voltages and temperature.

The solution to this problem is the four transistor CMOS Trans conductance element, whose operation resembles in most respect that of the CMOS inverter but without having PSR problems. Fig.7 shows the CMOS Linear Tunable Transconductance Element.The CMOS-LTE Comparator consists Linear Tunable Transconductance Element and an inverter. By systematically varying the transistor sizes of the CMOS linear tunable Trans conductance element,the internal reference voltages are generated. The transistor sizes of CMOS Transconductance are identical in this design, with Vg1 and Vg4 as fixed voltages. The output of this component is connected to CMOS inverter in order to increase the voltage gain of the comparator.

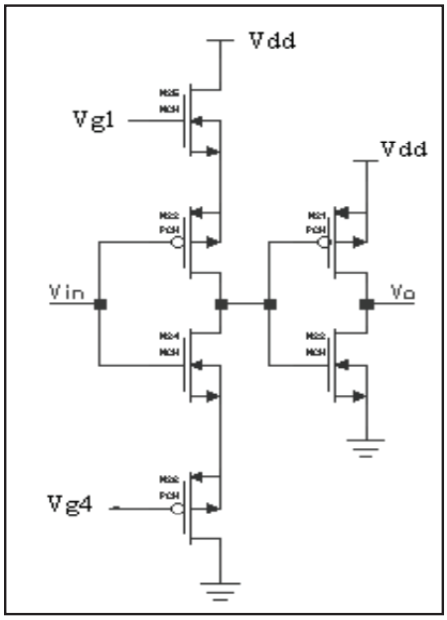


Fig. 7: CMOS-LTE Comparator

VII. Implementation and Results

A. Two Stage Open Loop Comparator (IN TANNER EDA Using 180NM Technology)

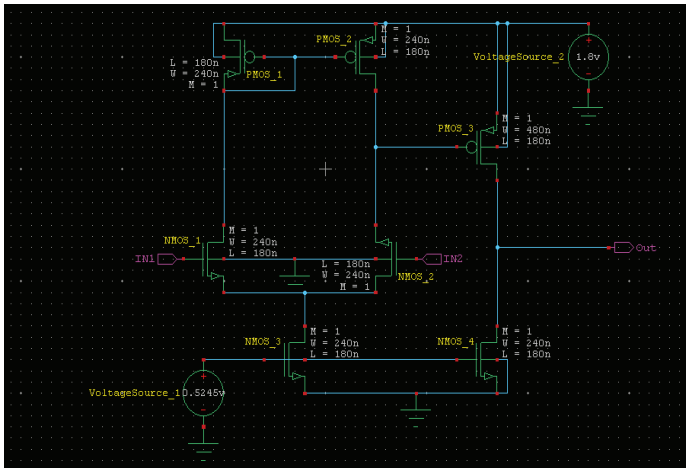


Fig. 8: Two Stage Open Loop Comparator

1. Transient Analysis

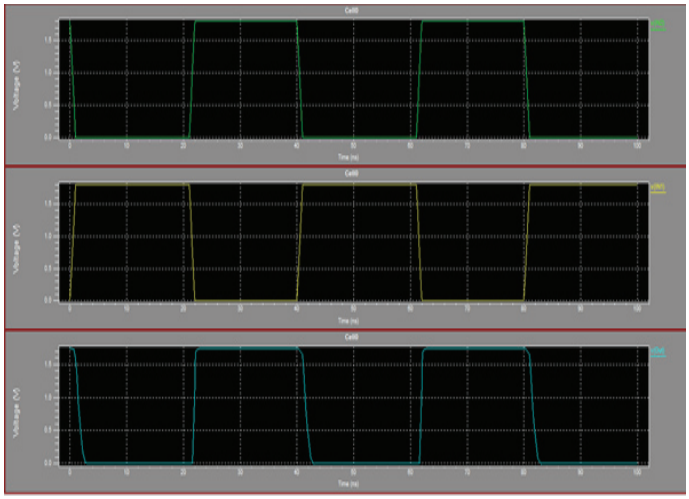


Fig. 9: Transient Analysis of Two Stage Comparator

2. Power Results (Open Loop Comparator)
VVoltageSource_2 from time 1e-008 to 1e-007
Average power consumed -> 2.370059e-005 watts
Max power 7.570612e-005 at time 4.1e-008
Min power 5.441084e-006 at time 2.1375e-008

3. Delay Analysis
tdlay = -1.8463e-008
Trigger = 4.0250e-008
Target = 2.1787e-008

B. Implementation of TIQ (Threshold Inverter Quantization using 180nm Technology)

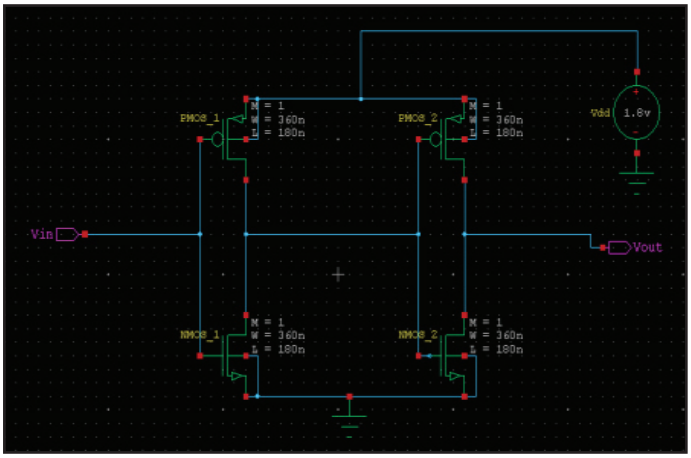


Fig. 10: Schematic of TIQ Comparator

1. Transient Analysis

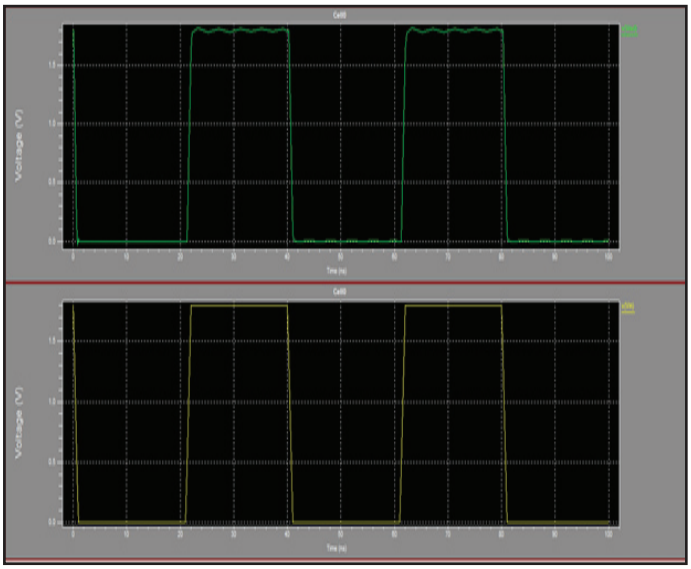


Fig. 11: Transient Analysis of TIQ

2. Power Results (TIQ comparator)
VVoltageSource_1 from time 1e-008 to 1e-007
Average power consumed -> 1.694443e-006 watts
Max power 6.135738e-005 at time 2.2e-008
Min power 1.548471e-007 at time 1e-008

3. Delay Analysis
tdlay = 2.0173e-010
Trigger = 4.0278e-008
Target = 4.0480e-008

4. Transistor Count = 4

C. Implementation of Quantized Differential Comparator

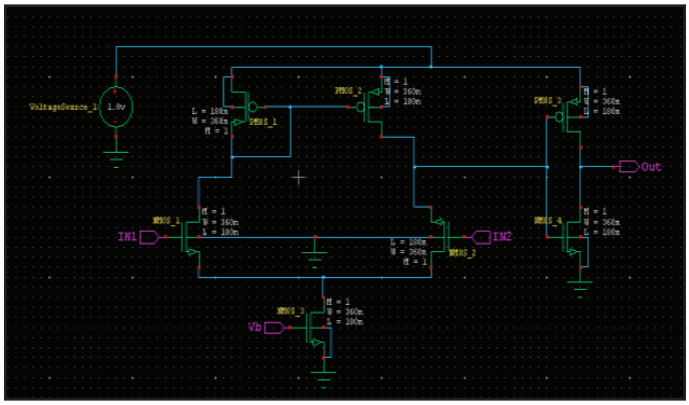


Fig. 12: Schematic of Quantized Differential

1. Transient Analysis

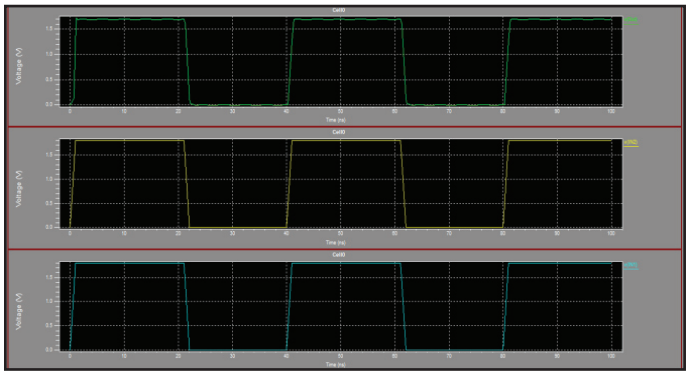


Fig. 13: Transient analysis of QDC Comparator

2. Power Results
VVoltageSource_1 from time 1e-008 to 1e-007
Average power consumed-> 1.594352e-004 watts
Max power 3.089151e-004 at time 8.1e-008
Min power 2.372884e-007 at time 4.025e-00

3. Delay Analysis
tdlay = 2.7083e-010
Trigger = 4.0278e-008
Target = 4.0549e-008

4. Transistor Count = 7

D. Implementation of Two Stage CMOS Amplifier with an Output Inverter

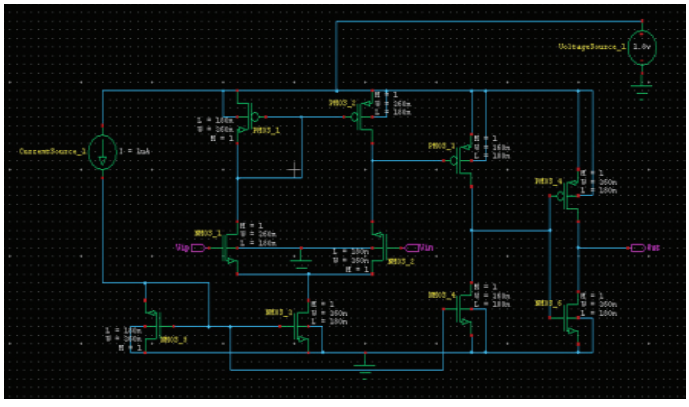


Fig. 14: Two stage CMOS amplifier with an output

1. Transient Analysis

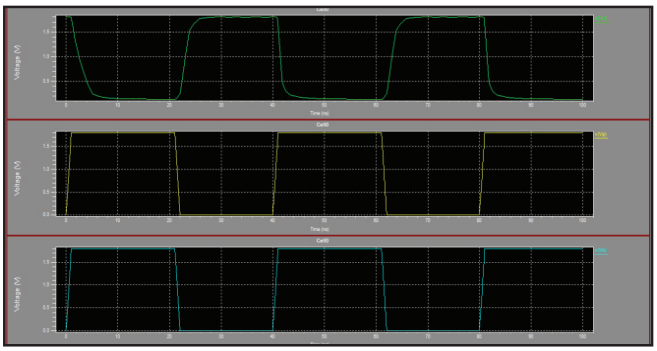


Fig. 15: Output waveform Inverter

2. Power Results

VVoltageSource_1 from time 1e-008 to 1e-007
Average power consumed -> 5.214885e-005 watts
Max power 9.352080e-005 at time 8.18344e-008
Min power 1.542141e-006 at time 7.27415e-008

3. Delay Analysis

tdlay = -1.7849e-008
Trigger = 4.0278e-008
Target = 2.2429e-008

4. Transistor Count = 10

E. Implementation of CMOS-LTE (Linear Tunable Transconductance Element) Comparator

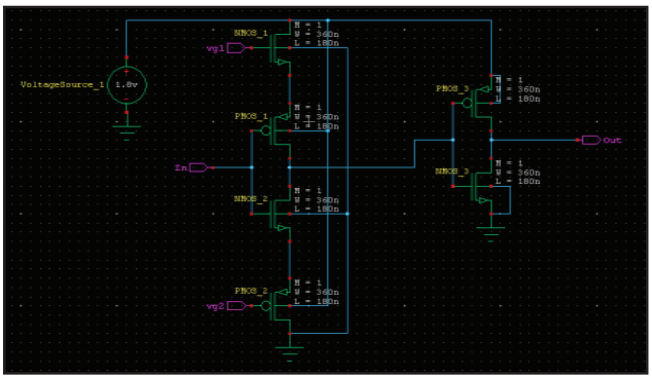


Fig. 16: Schematic of CMOS-LTE Comparator

1. Transient Analysis

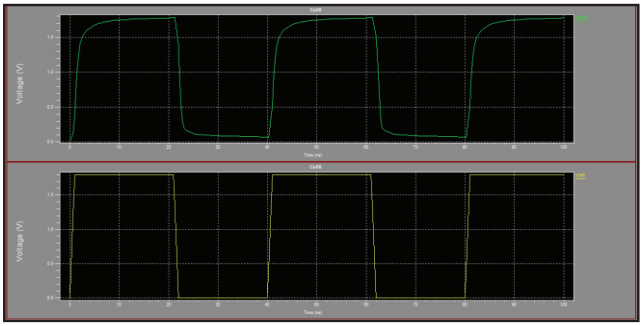


Fig. 17: Output waveform

2. Power Results

VVoltageSource_1 from time 1e-008 to 1e-007
Average power consumed -> 3.413433e-005 watts
Max power 8.273729e-005 at time 2.25336e-008
Min power 5.146837e-006 at time 2.1e-008

3. Delay Analysis

tdlay = 6.6778e-010
Trigger = 4.0278e-008
Target = 4.0946e-008

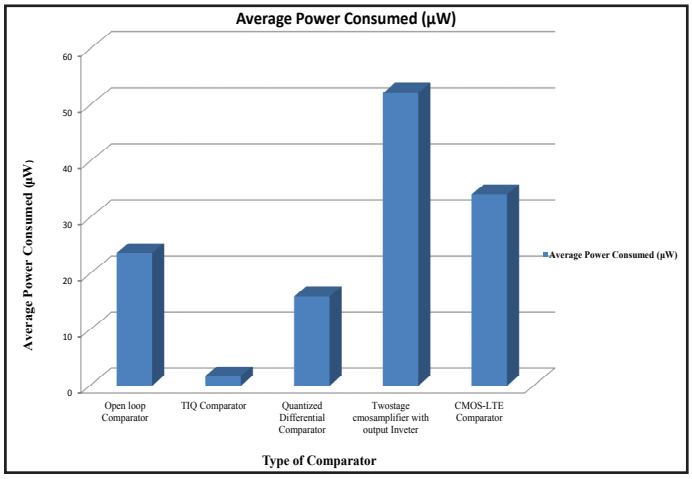
4. Transistor Count = 6

Table 1: Comparison

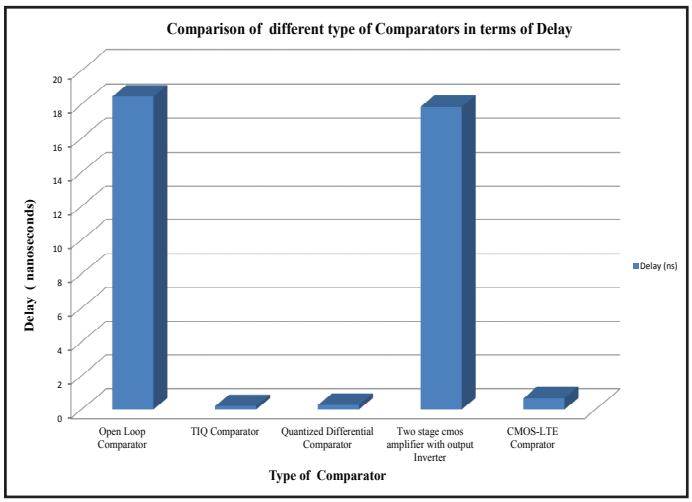
Comparator Type	Techno-logy	Transistor count	Average power Consumed	Delay	Power Delay Product (PDP)
Open Loop Comparator	180nm	7	2.370059e-005 watts 23.70059 µW	-1.8463e-008 -18.463 ns	437.50
Tiq	180nm	4	1.694443e-006 watts 1.694443 µW	2.0173e-010 0.20173 ns	0.338
Quantized Differential Comparator	180nm	7	1.594352e-004 watts 15.94352 µW	2.7083e-010 0.27083 ns	4.303
Two Stage Cmos Amplifier With Output Inverter	180nm	10	5.214885e-005 watts 52.14885 µW	-1.7849e-008 -17.849 ns	930.17
CMOS-LTE Comparator	180nm	6	3.413433e-005 watts 34.13433 µW	6.6778e-010 0.66778 ns	22.52

Graph:

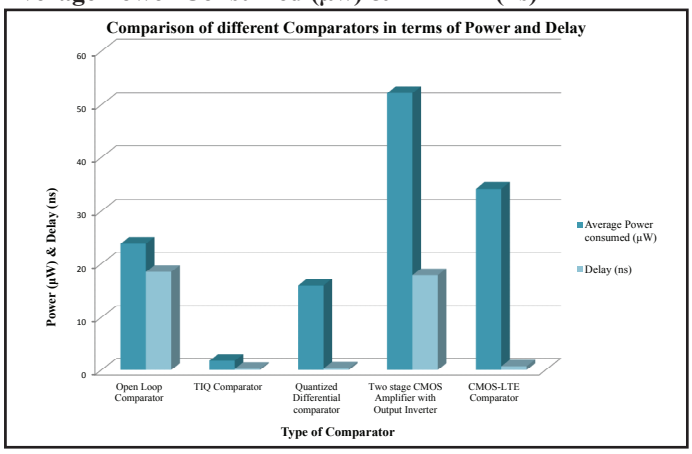
Average Power Consumed



Delay



Average Power Consumed (µw) & DELAY (ns)



VIII. Conclusion

In this paper, five comparator circuits have been designed. There are some disadvantages of TIQ comparator in some applications as stated in section 3. Two stage open loop comparator is presented using 180nm CMOS technology. After this a Quantized Differential Comparator has been implemented followed by a two stage Amplifier with Output Inverter and a CMOS-LTE Comparator. All these architecture can be extended from medium to high resolution applications because of the simplicity of the circuits. Comparators are a main part of analog circuits. As we can see in the power results that the average power consumed by TIQ comparator is less than that consumed by the open loop comparator and so is by quantized differential comparator. This is due to the reason that the TIQ comparator generates the reference voltage internally and hence the resistor ladder network is not required when designing a FLASH ADC. Quantized Differential Comparator can also be used for designing low power high speed Flash ADC's. The two stage CMOS amplifier with output inverter has also been implemented and the average power consumed by the circuit is calculated. Delay for all these circuits has been calculated and PDP has been defined which makes the comparison of all these circuits easier. As future work, we can design low power flash ADC using these comparator designs and a Priority Encoder.

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