Design of High Gain Low Voltage CMOS Operational Amplifier

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Abstract
This paper presents a design of High gain two stage CMOS operational amplifier, which operates at ±2.5V power supply using tsmc 1um CMOS technology. The OPAMP designed has two-stages and a single ended output and is designed to exhibit a gain bandwidth of 12MHz, gain of 81.52dB with a 62 degree phase margin and 45 degree gain margin to work with a load capacitance of 10pF and have power dissipation 0.7mW. The Operational Amplifier is designed using RC Compensation for stability. Design and Simulation has been carried out in P Spice.

Keywords
CMOS Op-Amp, Gain, Stability, RC Compensation, Slew Rate

I. Introduction

The Operational Amplifier (Op-Amp) is a very basic building block in Mixed Signal design. Basically, Op-Amps are voltage amplifiers being used to get high gain by applying differential inputs. The gain is typically between 50 to 60 decibels. Two stages Op-Amp is one of the most commonly used Op-Amp architectures. The continuously scaling of transistor size allows the more number of transistors on the same size of chip which reducing time delays [2]. This results in continuous increase in the processing capacity and operating frequency. Operational Amplifiers is used very commonly in electronic circuits. Op-Amp based circuits are more precise, noise insensitive and are less influenced to fluctuations. The big challenge is to Design a stable operational amplifier with a high gain and high gain bandwidth with reducing voltage supply and channel length. Trade off among various parameters such as power dissipation, bandwidth, speed, gain has to face while designing Op-Amp [1]. With higher gain and bandwidth the speed and accuracy of the amplifier increases but the stability in negative feedback decreases. One of the basic limitations of op amp is that they are not especially fast. The typical performance reduced rapidly for frequencies which are greater than about 1 MHz, although some models using different technique are designed specifically to handle higher frequencies [4]. To design a stable Op-amp with higher frequency always a big task. Aim is to build an Op-Amp with a fairly large gain and comparatively high unity gain bandwidth at a maximum phase margin and gain margin to ensure stability. Various compensation techniques can be adopted to achieve this. In this paper a two stage CMOS Op amp is designed with high gain and stability.

II. Two Stage CMOS OP AMP Architecture

The reduced channel length devices puts new challenges in designing of Op-Amps puts in low power applications with reduced channel length devices. Advancements which have appeared recently through new techniques and technologies, give us more alternatives in implementations. Two stage CMOS Op–Amps has two dominant poles the phase margin could e reach to less than the amount easily which is just enough for stable operation. The problem like this should be look by designers, otherwise there will be possibility that the output of Op-Amp will oscillate and it will become an oscillator instead of an amplifier. In some applications the gain and/or the output swings provided by cascade op-amps are not adequate. For these cases, we used "two stage" Op-Amps, with the first stage providing a high gain and the second, large swing. In amplifier employing the negative feedback frequency compensation technique is used to improve stability.

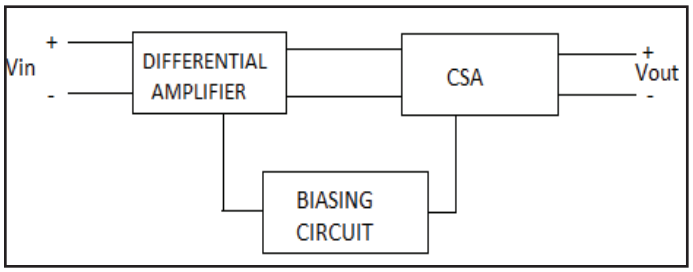

Fig. 1: Two Stage Operational Amplifier

Two stage operational amplifiers consist of a differential amplifier in the 1st stage followed by a Common Source Amplifier in the 2nd stage. Differential Amplifier stage is to ensure high gain and CSA stage is to further increase the gain an also provide high voltage swing at the output. The block diagram of a two stage CMOS Operational amplifier is shown in fig. 1. The 1st block is a differential amplifier. It has two inputs, non inverting input and inverting input. It can give a differential voltage or single ended voltage, decided by configuration at the output which depends on differential input voltage. Single ended output reduces the output swing of the amplifier. The Common Mode Rejection Ratio is also degrades as the symmetry of the circuit is lost.

The differential amplifier stage is not enough in some circuit, additional amplification required is provided by the second stage, which is the common source amplifier, and it is driven by the output of the differential amplifier stage. The biasing circuit incorporated to provide the proper operating point to each transistor in its saturation region [2]. At the end to provide the low output impedance, an output buffer stage can be attached and larger output current needed to drive the load. Output buffer is not required for a small capacitive load. When the output buffer stage is not used, the circuit becomes an operational transconductance amplifier or OTA.

III. Op-Amp Architecture

The circuit consists of three subparts: the differential gain stage, second gain stage and biasing circuit. MOSFETS M1, M2, M3, M4, M5 form the first stage which is differential amplifier stage. M6 and M7 form the second gain stage and are in Common Source Amplifier Configuration. M8 and the Current source form the biasing circuitry. M9 and the Compensation capacitor provide frequency compensation needed for stability. To make Op amp stable right hand pole is main concern. To remove the right hand pole we use rc compensation technique.

A. Differential Gain Stage

The differential gain stage consists of MOSFETS M1, M2, M3, M4 and M5 as shown in fig. 2. Positive input signal is applied to the gate of M1 and negative input is given to the gate of M2. An

active load which is a current mirror made up of M3 and M4 is used in this stage. The gain of first stage is the transconductance of M1 multiply by the total output resistance seen at the drain of M2. The output resistance is mainly contributed by the input transistors themselves and also the output resistance of the load transistors, M4 and M3. The active load current mirror used in this circuit has three main advantages. First, the chip area occupied is small and gives comparatively large output resistance. The current mirror provides the differential input to single- ended output, and finally, the load helps with common mode rejection ratio. In this, the differential input to single ended output is achieved by using a current mirror (M4 and M3). The current is mirrored by M3 and M4 from M1 and subtracted from the current from M2. Finally, the output resistance of the input stage is multiplied by differential current from M1 and M2 gives the single-ended output voltage, which is the part of the input to the next stage. The transconductance of this stage is simply the transconductance of M1 and M2.

$$g_{mI} = g_{m1} = g_{m2}$$

B. Common Source Amplifier Stage

The second stage consists of a common source amplifier which acts as a current sink load inverter. The aim of the second gain stage is to give additional gain and it consisting of transistors M6 and M7. The output of first stage is the input to this stage. It consists of a capacitor to move the pole which is lowest in frequency to higher frequency. Due to this movement of pole the stability of the amplifier is increased. For stability $C_C > 0.22C_L$.

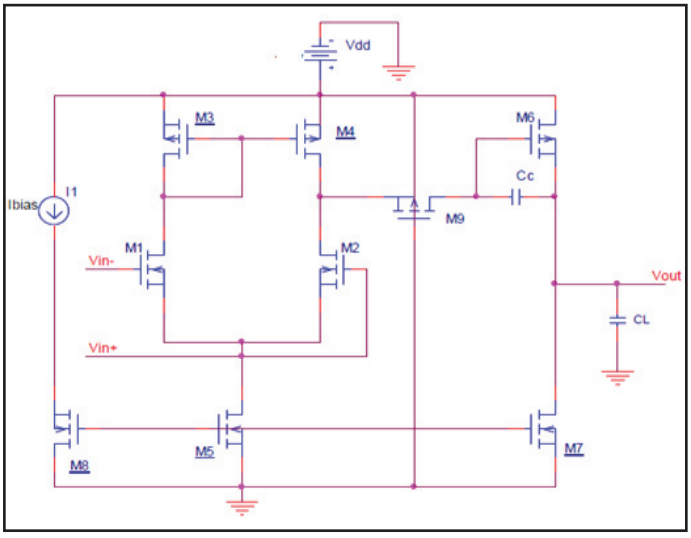

Fig. 2: Two Stage Op-Amp Circuit

M6 the common source amplifier amplifies the output comes from the drain of M2. M7 is active load transistor, which serve as the load resistance for M6 in this stage. This stage has gain which is the equivalent load resistance seen at the output of M6 and M7 multiplied by the transconductance of M6. M6 is the driver while M7 acts as load. The transconductance of this stage is the transconductance of M6.

$$g_{mII} = g_{m6}$$

C. Biasing Circuit

Current source, I1 in fig. 2 acts as a reference source for transistor M8. I1 and M8 form a current mirror biasing network driving the transistors, M5 and M7 which act as current sinks. The bias network controlled the gate to source voltage of M5 and M7. Biasing is needed to make all transistors to work in saturation region. If we increase the size of M5, slew rate and phase margin will be increase.

D. RC Compensation

R and Cc are used between gate and drain of M6 to improve the phase margin and hence stability of the circuit. For this purpose instead of resistance a MOS transistor is used.

IV. Design of the Two Stage Op AMP

The first point considered in the design was to meet the desired specifications. Based on a clear understanding of the specifications, the standard CMOS Op-Amp circuit topology in this design has been chosen.

Table 1: Specification of two-stage CMOS op-amp

Specification Names	Values
Supply Voltage	± 2.5V
Gain	> 80db
Gain Bandwidth	≥ 10Mhz
Slew Rate	20V/µSec
Output Swing	± 2.5V
Common Mode Rejection Ratio	> 60db
Phase Margin	≥ 60°
Power Dissipation	≤ 1mW
ICMR	-2.5V To +2.5V

A. Design Methodology

The DC gain of the first stage is

$$A_1 = -\frac{g_{m2}}{g_{ds2} + g_{ds4}}$$

The DC gain of the second stage is

$$A_2 = -\frac{g_{m6}}{g_{ds6} + g_{ds7}}$$

Overall gain of the Op-amp is

$$A_V = A_1 . A_2$$

$$A_V = \frac{g_{m1} g_{m6}}{(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}$$

Slew Rate of the Op-amp is

$$SR = \frac{I_5}{C_C}$$

Where I_5 is the current through the M5 transistor and it is the bias current of the input stage.

The Gain bandwidth of the Op-Amp is

$$GB = \frac{g_{m1}}{C_c}$$

V. Simulation Result

A. DC Sweep

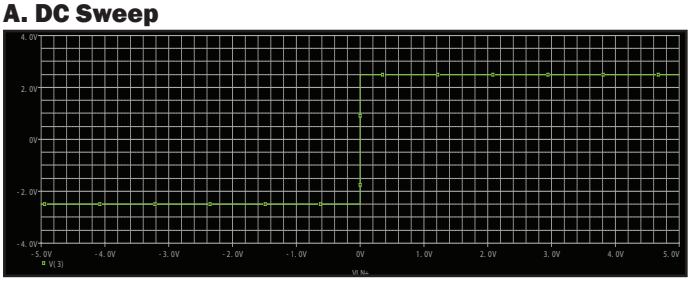

Fig. 3: Open Loop Transfer Characteristics

B. Frequency Response

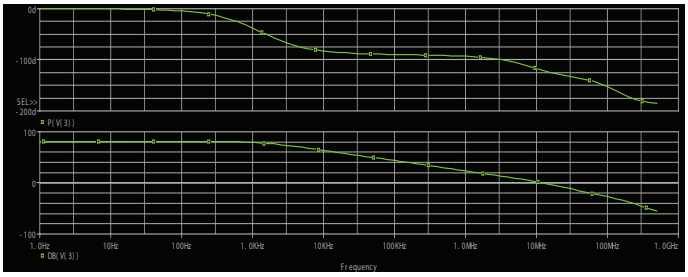

Fig. 4: Frequency Responses

C. Common Mode Gain

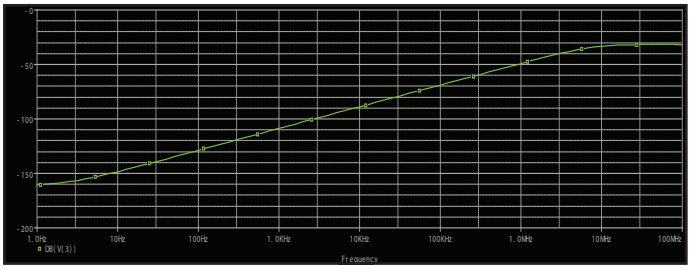

Fig. 5: Common Mode Gain

D. ICMR

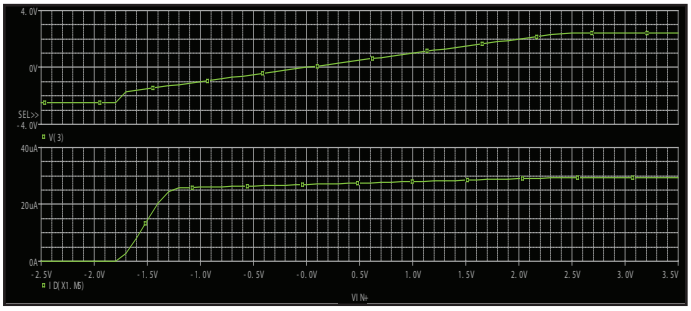

Fig. 6: Input Common Mode Range

E. Transient Analysis

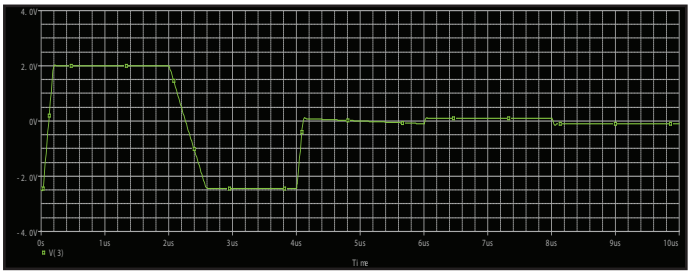

Fig. 7: Transient Responses

Table 2: The Geometric Dimension Incorporated and the Electrical Parameter Yielded

The Design Parameters		The Electrical Parameters Yielded	
M1	3/1 um/um	Phase margin	62°
M2	3/1 um/um	Gain	81.51db
M3	15/1 um/um	C_C	1Pf
M4	15/1 um/um	UGB	12MHz
M5	4.5/1 um/um	ICMR	-1.2 - 2.5V
M6	94/1um/m	Slew Rate	27.87V/us
M7	14/1 um/um	Common Mode Gain	-150db
M8	5.1/1 um/um	Output Swing	± 2.5V
M9	1/1 um/um	Gain Margin	45°
I_{BIAS}	30uA	Power Dissipation	0.7mW
V_{DD}	2.5V	Output Resistance	138.6kΏ
C_L	10PF	3db frequency	1KHz

VI. Conclusion

This paper presented the full design and analysis of a two stage CMOS Op-Amp. The amplifier presented in this paper operates in saturation mode and regulates its bias current. When a signal is applied the current in the amplifier increases so that these amplifiers have very high driving current. The Op-Amp has low power as well as low voltage. RC compensation is used for stability which makes Op-Amp quite stable. But there is always some scope of improvement, here we can increase gain bandwidth more with open loop gain.

References

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Shahid Khan received his B.Tech degree from B.S.A College of Engineering & Technology in Electronics & Communication in 2009. His research areas include Analog VLSI Design and Communication engineering.

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