Study of Implementation of Vedic Math's Sutras in Designing of Multipliers

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Abstract

In present era the importance of fast and accurate devices is on high. The ALU is a most important part of processing devices. The speed of ALU can improve by using more fast and précised multipliers. Vedic math's is playing important role in designing a multipliers. The study of Urdhva-tiryakbhyam Sutra, Nikhilam Sura, and Booth Multiplier revels that Nikhilam Sutra is having advantage edge over other technologies. The process delay or speed of multiplication is found improved by approx 20% using Nikhilam Sutra. The use of Nikhilam Sutra of Vedic Math's not only improves the performance of ALU but it makes it small in size and more power efficient.

Keywords

4:2 Compressor, 7:2 Compressor, Booth's multiplier, high speed multiplier, modified Booth's multiplier, Urdhwa Tiryakbhyam Sutra, Vedic Mathematics

I. Introduction

With the rapid advancement in technologies, the demand of faster devices is increasing. Same is going in electronics, where the demand of integrated circuits capable of faster processing is growing. To make faster the process of processor IC's a simple way is to improve the response time of arithmetic logic unit. Arithmetic operations such as addition, subtraction, and multiplication can be use to enhance the speed of computation [1].

In the last few years many researchers have found that Indian Vedic math's sutras can be helpful in reducing the response time of a multiplier. A multiplier is one of the key hardware blocks in most of applications such as digital signal processing encryption and decryption algorithms in cryptography and in other logical computations [2]. Multiplier is the core component of any DSP applications and hence speed of the processor mostly depends on multiplier design [2].

Before starting comparative study, one should know what is Vedic Mathematics and from where it started from. Vedic mathematics is an ancient method of solving mathematical problems; it was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884-1960), a scholar of Sanskrit, mathematics, history and philosophy. He studied these ancient texts for years and, after careful investigation, was able to reconstruct a series of mathematical formulae called sutras [3]. There are total 16 sutras, who defines the calculation process in

- 1. Anurupye Shunyamanyat -If one is in ratio, the other is
- Chalana Kalanabyham -Differences and similarities.
- 3. Ekadhikina Purvena- By one more than the previous One.
- 4. Ekanyunena Purvena -By one less than the previous one.
- Gunakasamuchyah-Factors of the sum is equal to the sum
- 6 Gunitasamuchyah-The product of sum is equal to sum of the product.
- Nikhilam Navatashcaramam Dashatah -All from 9 and last

- Paraavartya Yojayet-Transpose and adjust.
- Puranapuranabyham -By the completion or noncompletion.
- 10. Sankalana- vyavakalanabhyam -By addition and by subtraction.
- 11. Shesanyankena Charamena- The remainders by the last
- 12. Shunyam Saamyasamuccaye -When the sum is same then sum is zero.
- 13. Sopaantyadvayamantyam -The ultimate and twice the penultimate.
- 14. Urdhva-tiryakbhyam -Vertically and crosswise.
- 15. Vyashtisamanstih -Part and Whole.
- 16. Yaavadunam- Whatever the extent of its deficiency.

The above given sutras can use for making different mathematical calculations simpler and faster. The process of multiplying two quantities using usual method is comprised of number of steps which make it bulky to realize, time consuming in processing, and high power consuming. For solving the same problem researchers have suggested various solutions. Use of vedic math's sutras are some commonly accepted methodologies by researchers for optimizing the VLSI multiplier designs.

Most common Vedic math's sutras in designing of multiplier are Nikhilam and Urdhva-tiryakbhyam.

In this paper we present a comparative study among different multiplier designing approaches.

II. Urdhva-tiryakbhyam Sutra

The Urdhv triyankbhyam Sutra of vedic maths can be utilize for enhancing the speed of multiplication operation. An example of multiplication using Urdhva-triyakbhyam sutra is given below:

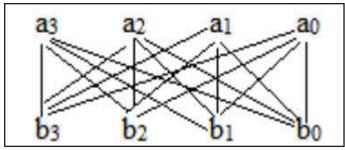


Fig. 1: Example of 4x4 Multiplication using Urdhva-triyakbhyam

For multiplying 4x4 strings using conventional method four partial products are to be added which make the process and design bulky, where as in multiplier using Urdhva-triyakbhyam sutra only single step addition is required, which make adding process faster and system smaller in size. The detailed method of multiplication using Urdhva-triyakbhyam sutra can be explained as shown in fig. 2.

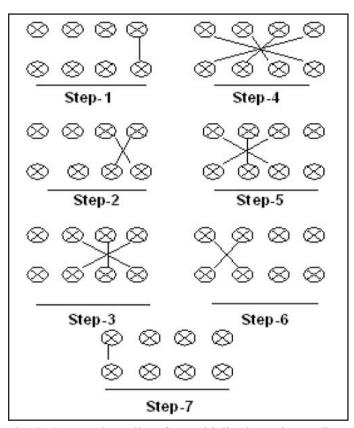


Fig. 2: Steps to be Follow for Multiplication using Urdhvatriyakbhyam Sutra

As shown in fig. 2 for multiplying two strings first vertical elements of strings are to be multiply and then cross elements are multiply followed by addition of results.

III. Nikhilam Sutra

The As above discussed the multiplication of two number strings is a tedious task, but using vedic math's sutras this could be simplified. The Urdhva-trivakbhyam sutra may grately simpligy the process of multiplication and reduces the steps and size of device used as well. But with the help of Nikhilam sutra problem may further be more simplified and the number of elements may

Nikhilam Sutra factually means "all from 9 and last from 10". Although it is valid to all cases of multiplication, it is more capable when the numbers involved are big. Since it checks out the compliment of the large number from its adjacent base to perform the multiplication operation on it, better is the original number, lesser the complexity of the multiplication. We first illustrate this Sutra by in view of the multiplication of two decimal numbers (92 * 98) where the chosen base is 100 which is nearest to and greater than both these two numbers

Answer is 9016

A. Multiplication Using Nikhilam Sutra

As The right hand side (RHS) of the product can be attained by just multiplying the numbers of the Column 2 (8*2 = 16). The left hand side (LHS) of the product can be found by cross subtracting the succeeding number of Column 2 from the initial number of Column 1 or vice versa, i.e., 92 - 2 = 90 or 98 - 8 =90. The concluding result is attained by concatenating RHS and LHS (Answer = 9016).

IV. Barrel Shifter

Barrel Shifter is an important part of ALU of a processor. The shifter is used to perform shift right, shift left, and rotational operations. Barrel shifter is designed using Mux trees to use it in repetitive form so that power consumed by the barrel shifter should minimum [4].

Multiplexer is used as a basic building block for a barrel shifter. The required number of multiplexer for any barrel shifter can be calculate using following formula [4]

Number of Multiplexers = $(No. of Bits)* log_2 (No. of Bits)$

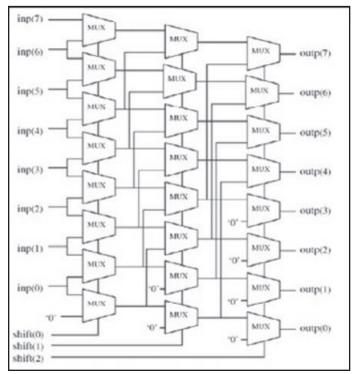


Table 1: Comparison for 4x4 multiplier [7]

Sr. No.	Technology	Path Delay	Power Consumption
1	Urdhvatiryakbhyam Sutra	15.095	0.085 W
2	Nikhilam Sutra	20.296	0.084 W
3	Booth Multiplier	19.66[5]	0.09 W

V. Conclusion

It may be conclude from above study that use of Nikhilam Sutra is advantageous over other algorithms. The speed of working seems to be improve by 33% and number of component is reduced by 20% approximately. The number of component is directly proposnal to the size and power consumption in chip, which means that these two factors are also improvised by using Nikhilam Sutra.

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