Design of Low Voltage Current Feedback Operational Amplifier

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Abstract
A new design of Low voltage Current Feedback Operational Amplifier (CFOA) based on second-generation positive current conveyor and opamp has been presented in this paper. By employing opamp at the output stage, the design overcomes the problem of achieving large transimpedance in low voltage circuits.
The design is implemented using 180nm technology process and the working of the proposed CFOA has been verified using PSpice simulations. It is shown that the developed CFOA has better slew rate and uses less transistors as compared to conventional design.

Keywords
Current Feedback Operational Amplifier (CFOA), Second Generation Positive Current Conveyor (CCII+), Voltage Feedback Amplifier (VFA)

I. Introduction

CFOA is a transimpedance amplifier which produces an output voltage proportional to input current. It is represented as a four-terminal network as shown in fig. 1 which has matrix of the following form.

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \\ I_o \end{bmatrix}$$

CFOA started getting attention of researchers working in analog and mixed signal design when it was realized that it can act as an alternative to conventional VFA mainly because of its independent gain-bandwidth product and high slew rate, which are not inherent in VFA. Its high slew rate makes it ideal for high frequency applications, whereas gain bandwidth independence allows designers to operate over wide range of frequency without compromising with gain. These features make CFOA more preferable over the conventional voltage amplifiers.
Various architectures have been proposed to design CFOA [1-6], but they typically use CCII+ and buffer [4-6] as shown in fig. 2. However, the limitation in the use of cascode transistors at the Z node of the CCII+ in low voltage designs can severely restrict the available transimpedance of the overall CFOA, thereby reducing its performance [8].
In this paper, the opamp based approach introduced in [8] has been used to design CFOA, as it does not require the transimpedance to be large. This happens because the gain impedance gets shifted to an additional opamp, thereby making it attractive to work for low voltage design [8].
This paper is organized as follows. In section II, the design methodology which has been used to design proposed circuit is explained. In section III, the detailed description of proposed CFOA and its CMOS realization are given. In section IV, PSpice simulation results of the proposed circuit using CMOS 180nm technology are illustrated. In section V, conclusion is drawn.

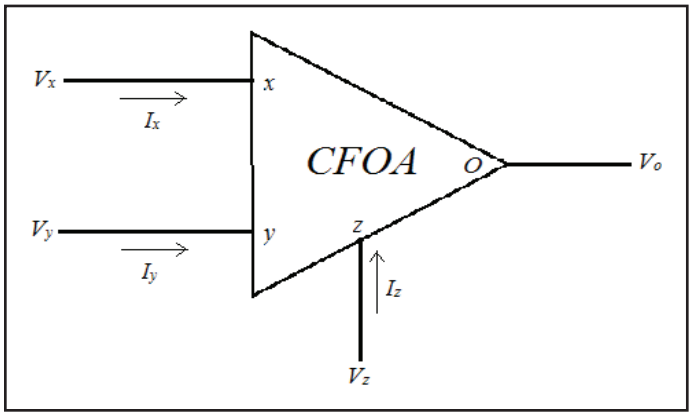

Fig. 1: Current feedback opamp symbol

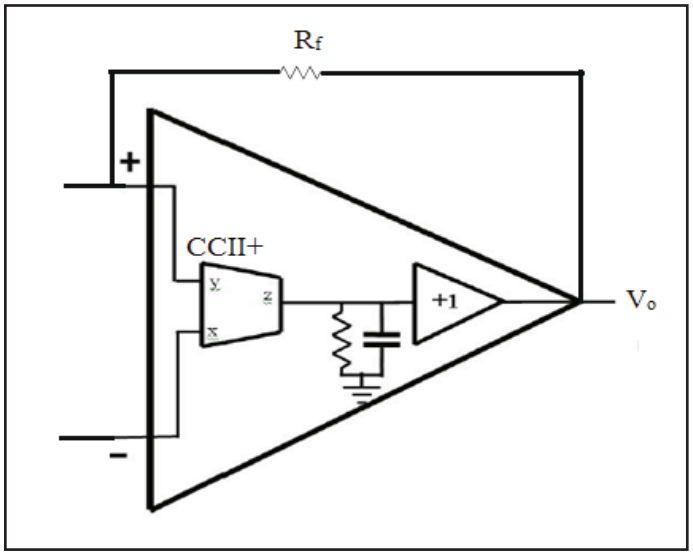

Fig. 2: Conventional CFOA made using CCII+ and voltage buffer

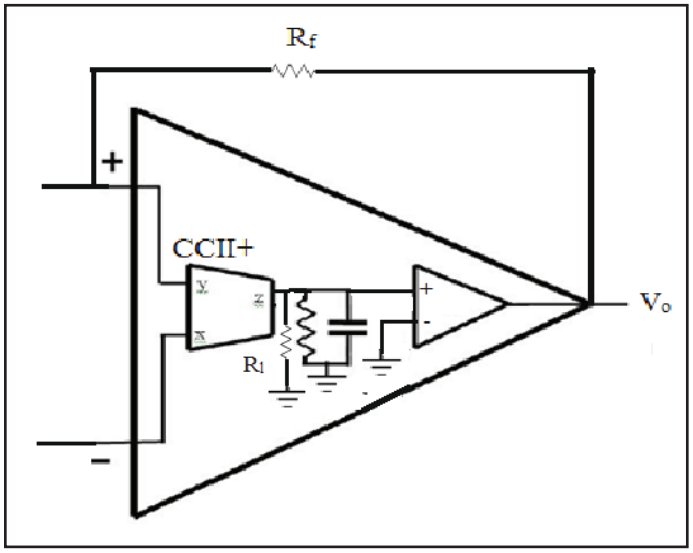

Fig. 3: CFOA made using CCII+ and opamp

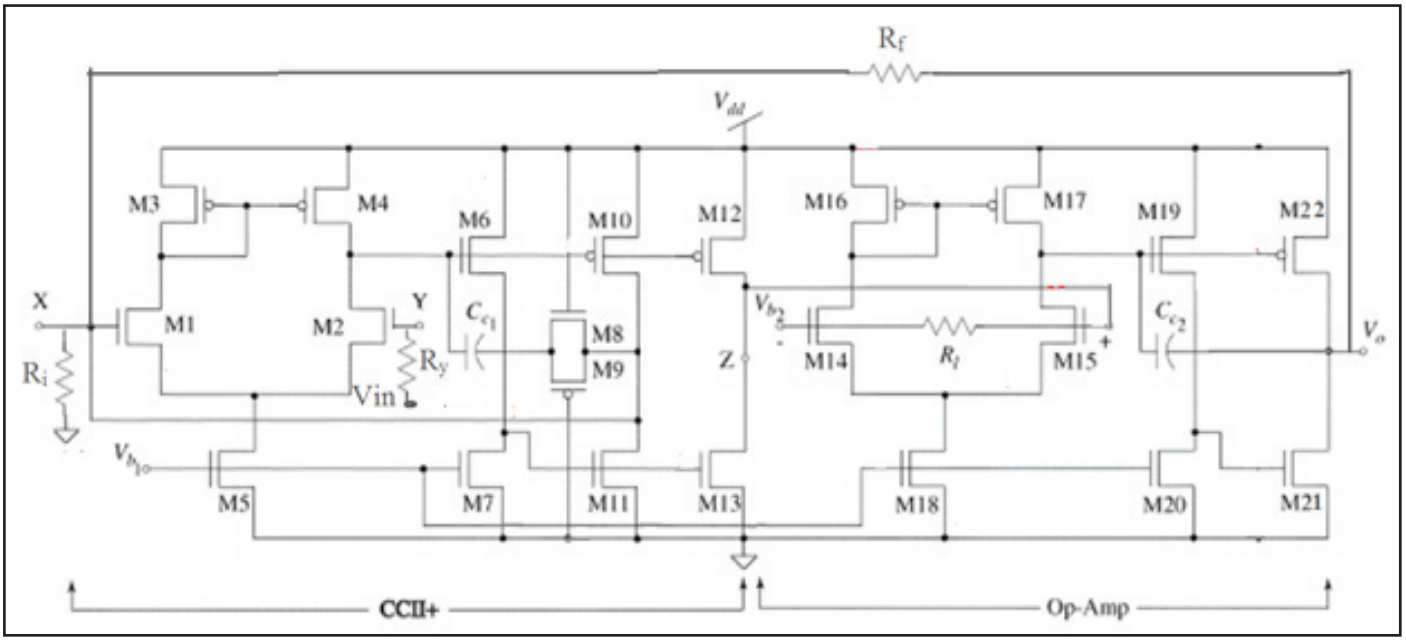

Fig. 4: Circuit diagram of proposed CFOA

II. Design Methodology

The approach which has been used to design CFOA is shown in fig. 3. It uses opamp in open loop configuration to achieve high overall transimpedance.The opamp used at the output stage transfers the high voltage swing at the Z node of CCII+ to the output node of CFOA. To achieve this, the output current of CCII+ is converted into voltage by an additional resistor R_l, which is further connected to the non-inverting input of opamp. The converted voltage is then amplified by opamp.

The straight forward small signal analysis carried out in [8] of the model given in fig. 3 shows that the bandwidth and gain of transimpedance amplifier are proportional to R_l / R_f and R_f / R_i respectively, where R_l is the load resistor, R_f is the feedback resistor and R_i is the input resistor. Therefore, for a particular feedback resistor, gain and bandwidth can be controlled independently by selecting appropriate R_i and R_l. Furthermore, the slew rate is regulated by the opamp which should be appropriately designed to achieve a high value.

III. Proposed Circuit of CFOA

The circuit diagram of the proposed CFOA is shown in fig. 4. It uses two stage conventional voltage opamp in closed loop configuration and an additional pair of transistors to design CCII+. Transistors M1, M2, M3 and M4 serve the purpose of differential amplifier whereas M6, M7, M10 and M11 form the class AB buffer stage which provides low output impedance and high output current needed for CCII+. The capacitor C_{c1} along with M8 and M9 are used to provide Miller compensation. Additional transistors M12 and M13 are used for current copying. The design of CCII+ made using this technique has already been covered before in [7].

The output stage of opamp is made using the same VFA which was used in the first stage, but the transmission gate coupled to C_{c2} is removed. It was observed that absence of transmission gate in the output stage affected the output characteristic slightly, but it was improved by changing the aspect ratio of the transistors employed in the design.

The aspect ratios of different transistors are given in Table 1 and the values of bias voltages and different passive components used inside the proposed circuit are specified in Table 2.

Table 1: Aspect Ratio of Transistors

Transistor	W/L Ratio	Transistor	W/L Ratio
M1	100/1	M12	60/1
M2	100/1	M13	20/1
M3	40/1	M14	80/1
M4	40/1	M15	80/1
M5	20/1	M16	46/1
M6	45/1	M17	46/1
M7	10/1	M18	15/1
M8	2.7/1	M19	45/1
M9	5/1	M20	10/1
M10	60/1	M21	65/1
M11	20/1	M22	1.1/1

Table 2: Component Values

Component	Value
R_i	1.5Kohm
R_f	1.5Kohm
R_l	1Kohm
R_y	1Kohm
V_{b1}	700mV
V_{b2}	900mV
C_{c1}	0.5pf
C_{c2}	4.5pf

IV. Simulation Results

The performance of the proposed CFOA circuit was verified by performing PSpice simulations with supply voltages 1.8V using 0.18μm TSMC CMOS technology parameters.

The transient and D.C. analysis of the CFOA were carried out to verify its four terminal equations:

$$I_x = I_z,\ I_y = 0,\ V_x = V_y,\ V_z = V_o$$

During D.C. analysis, a D.C. voltage of 1V was applied at Y terminal through resistor R_y and X terminal was connected to ground through R_i. The results of D.C. simulation are shown in fig. 5, 6 and 7. Fig. 5 shows the variation of voltage at X terminal of CFOA with respect to its Y terminal. Fig. 6 shows the variation of current at X terminal, Z terminal and Y terminal with respect to input voltage. Fig. 7 illustrates the variation of Vz and Vo with respect to input voltage. For transient analysis, pulse voltage source of 1V having time period of 100ns was used and analysis was performed for 200ns. Fig. 8, 9 and 10 show the results of transient simulation for V_x vs. V_y, I_x and I_y vs I_z and V_z vs. V_o respectively. Fig. 11 shows the calculation of slew rate of designed CFOA from output transient curve.

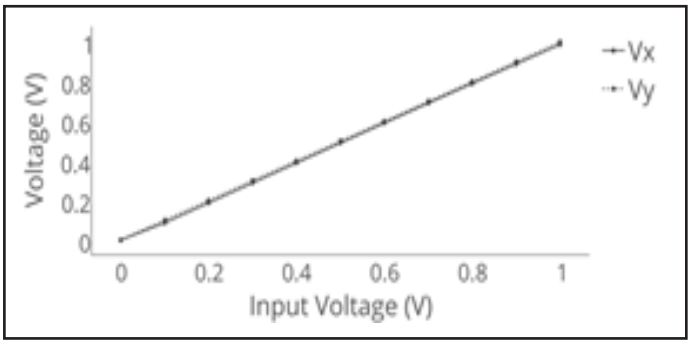

Fig. 5: D.C. Analysis verifying $V_x = V_y$

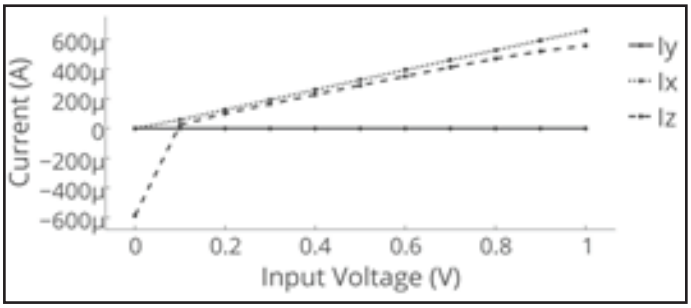

Fig. 6: D.C. Analysis verifying $I_x = I_z$ and $I_y = 0$

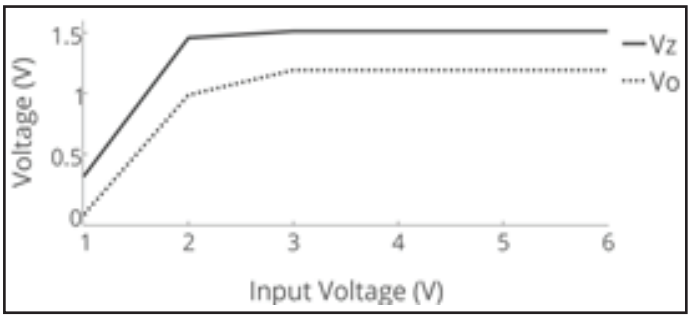

Fig. 7: D.C. Analysis verifying $V_z = V_o$

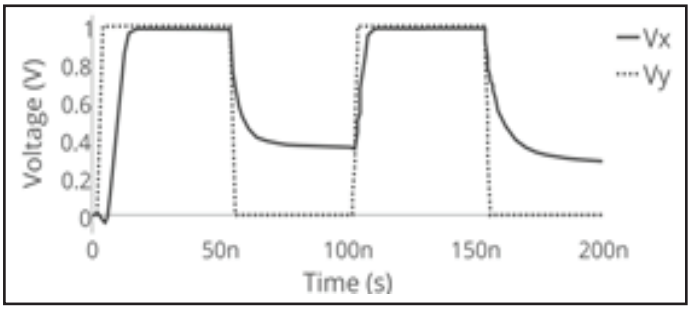

Fig. 8: Transient Analysis verifying $V_x = V_y$

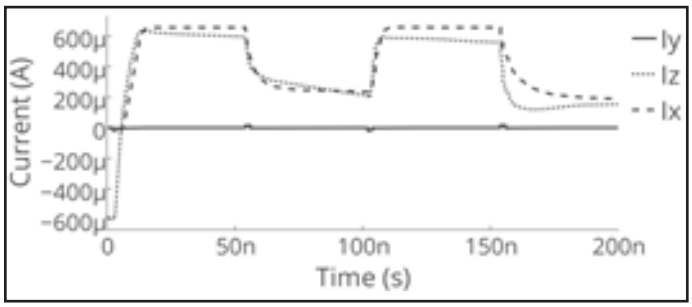

Fig. 9: Transient Analysis verifying $I_x = I_z$ and $I_y = 0$

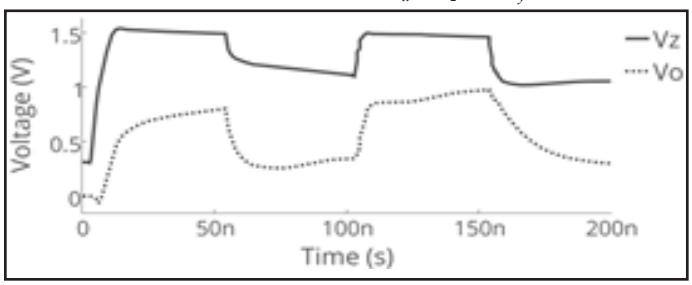

Fig. 10: Transient Analysis verifying $V_z = V_o$

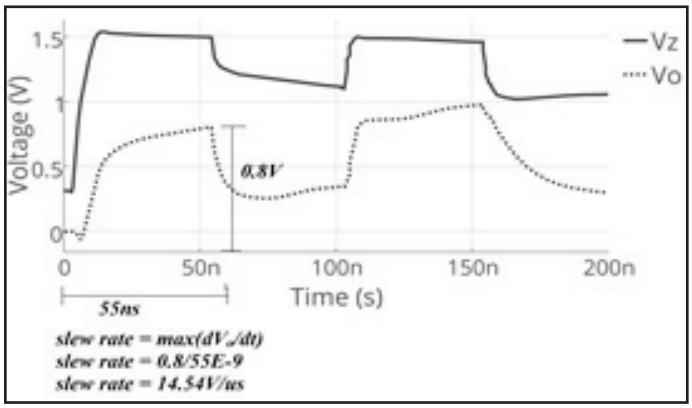

Fig. 11: Calculation of slew rate from output transient graph

V. Conclusion

A new design of CFOA based on opamp and CCII+ was presented and simulated using PSpice. As expected in simulations, the new CFOA has a higher slew rate (14.54V/µs) as compared to 8.75V/µs of the conventional one [8] despite using less transistors. Although the proposed CFOA block is suitable for low-voltage and low-power applications, it requires further exploration to enhance its gain and slew rate even further using some of the techniques presented in [9-12].

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