Study of Power Consumption Using the Schematic and Layout Designing of a 4*4 Wraparound Barrel Shifter

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Abstract
In modern Digital Signal Processing (DSP) applications the shifter is an important module of the processors. Thus the focus of this paper is to design the 8*8 wrap around barrel shifter using pass transistor logic [1]. It is a fundamental element of an ALU. In our proposed model the Barrel Shifter is used to design shifting operation in left to right direction. The design of our proposed circuit is done by Tanner EDA 13.2 tool and layout of the circuit is done by Credence tool. In our work we have evaluated VLSI parameters on different submicron technologies and obtain 45% reduction in power consumption in 16 nm technology compared to 22 nm.

Keywords
Barrel Shifter, Different Sub micron Technologies, Optimized Layout

I. Introduction

With the advancement towards the ultra-submicron technology, digital circuit designs are increasingly becomes more complex but it leads towards a better performance in VLSI parameters. Shifter is a fundamental integral part of a digital circuit designs. There are many applications where shifter plays a vital and important role. Some common usage of a shifters is in field of the hardware implementation of floating-point arithmetic (like additions, subtractions, normalizations), address generations, field extractions, variable length coding, word packing and unpacking [2].

A barrel shifter is well-known logic architecture. The main function of this digital circuit is to provide the left- or right- shifting of digital words. It can be designed using sequences of multiplexers. Additionally, a barrel shifters also provide zero-filling, and wrap-around processing for a digital processor.

In this paper we have presented a 4*4 wrap around barrel shifter. Here we have performed logical right shift operation the output in different submicron technologies. We have analyzed the power generated by the circuit in each technology and designed the layout of the circuit in 16 nm technology.

The reminder of this paper is divided into six parts. Section II elaborates the working principle of our proposed model. Section III describes the property of barrel shifter with respect to truth table also with the help of graph plots. Section IV elaborates the analysis of results in different submicron technologies of our proposed model and concludes the output values as a result. Section V highlighted most optimum layout with the respect of minimum power and minimum area of our proposed model in 22nm.

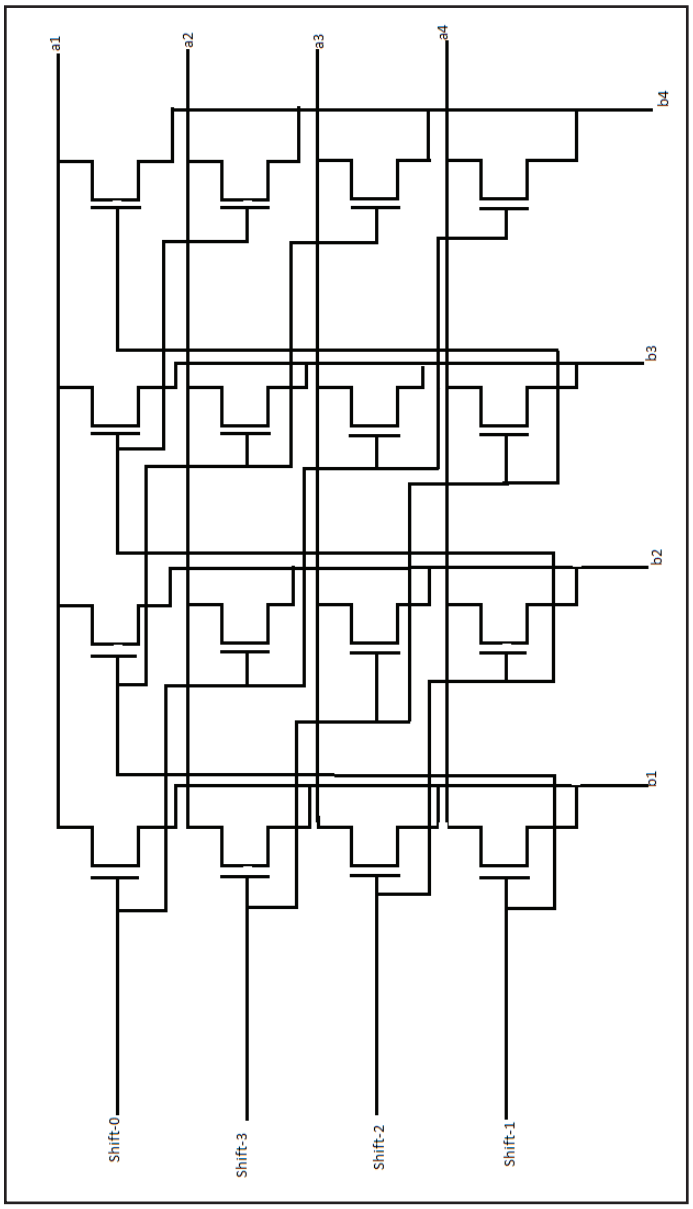
II. Theory of Barrel Shifter

A barrel shifter is known as wraparound or end around shifter. It is used as a switch array in a combinational logic design circuits. In a 4*4 barrel shifter there are 4-bit control buses running horizontally, and 4 bit input data buses running vertically. In each input buses shift controls are connected with a voltage source to supply proper bit source and get proper output curve. During the time of Shift-0 operation only four N-MOS are connected as an active MOS while others are connected to ground. If we connect an input level as Ai, shift controls as Si then the output obtained as Bi maintaining the Table 1.

III. Designing of Tanner EDA Tool

Initially we have design our circuit with the help of tanner simulator as shown in figure 1. The simulation wave form for the different shift operation is discussed in the subsection as given below. We have developed the structure in different sub-micron technologies to obtain an efficient power measurement. We analyzed our circuit in four of submicron technologies (16, 22, 32, 45), where we obtained the minimum power in 22nm [3].

The proposed model is:

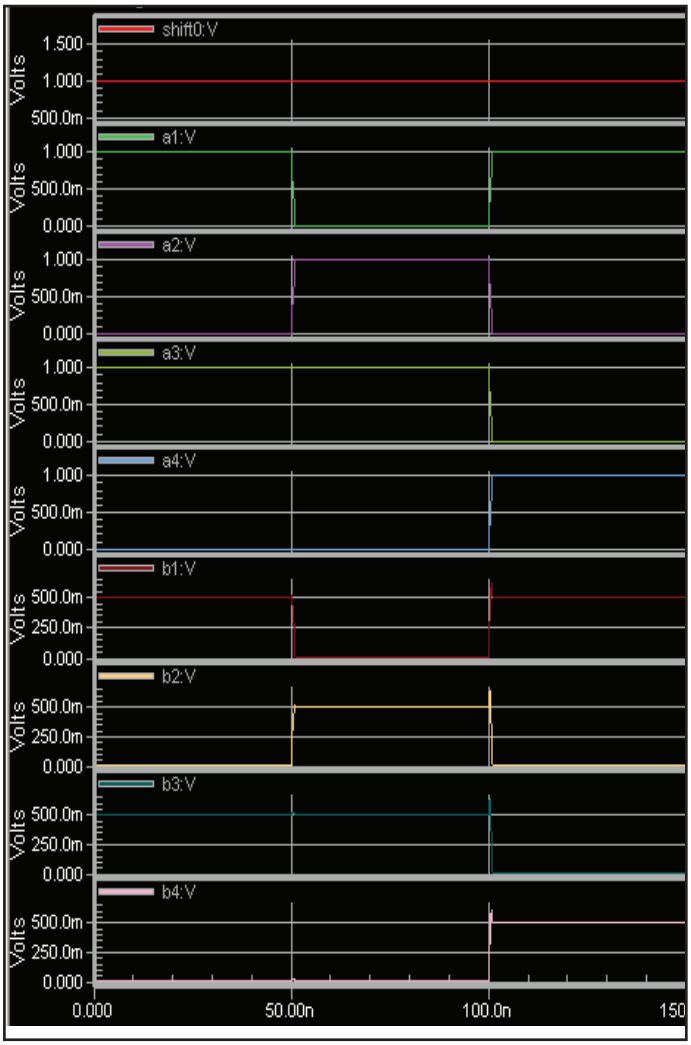


Here 16 N-MOS are used, in 4-input line as a1to a4 and 4-output lines from b1to b4 here also we are having 4-shifting operation from shift-0 to shift-3 as shown in table1 [4].

Control line			Connections
(s=0)	Shift 0 = 1 ,	all others=0	$a_1 \rightarrow b_1$, $a_2 \rightarrow b_2$, $a_3 \rightarrow b_3$, $a_4 \rightarrow b_4$
(s=1)	Shift 1 = 1,	-do-	$a_4 \rightarrow b_1$, $a_1 \rightarrow b_2$, $a_2 \rightarrow b_3$, $a_3 \rightarrow b_4$
(s=2)	Shift 2 = 1,	-do-	$a_3 \rightarrow b_1$, $a_4 \rightarrow b_2$, $a_1 \rightarrow b_3$, $a_2 \rightarrow b_4$
(s=3)	Shift 3 = 1,	-do-	$a_2 \rightarrow b_1$, $a_3 \rightarrow b_2$, $a_4 \rightarrow b_3$, $a_1 \rightarrow b_4$

According to this table the control line and cross ponding the connections lines shows that at a time one control line should be active and others remaining grounded. In this way we get the proper input - output graph which matches the truth table. The graphs are shown below

Graph for Control Line S=0



From the above graph is only for Shift-0, where the input output connections are same as truth table like a_1-b_1, a_2-b_2, a_3-b_3, a_4-b_4.

Similarly From the Graph for Control line S-1 the status is:- Here shift-1 is active high and others control lines are grounded. In this operation the value of input signal is shifted by one bit like a_1-b_2, a_2-b_3, a_3-b_4, a_4-b_1.

Similarly from the graph of control line S-2 the status is :- Here only shift-2 is active high others are remaining grounded. In this operation input values are shifted two bits towards output values as a result we get a_1-b_3, a_2-b_4, a_3-b_1, a_4-b_2.

Similarly from the graph of control line S-3 the status is :- Here only shift-3 is active high others control lines are remaining grounded. In this operation input values are shifted by three bits towards output values, as a result a_1-b_4, a_2-b_1, a_3-b_2, a_4-b_3.

IV. Analysis

We have analyzed our circuit in different sub-micron technologies to obtain power result. According to the Table 2 the minimum power is obtained in 16nm technology. To analyze the area requirement we have designed the layout using Credence tool as discussed in the next section. Here the values are also shown by table format

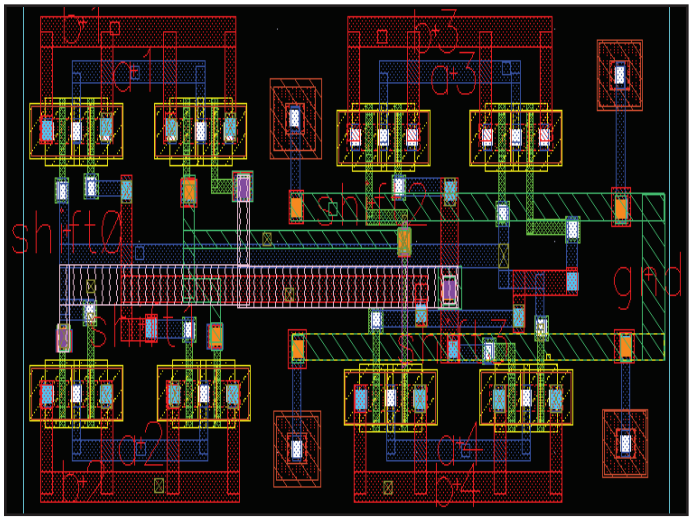
Table 1:

Technology	Power(w)
16nm	2.55
22nm	4.64
32nm	4.44
45nm	3.72

V. Layout

We made the layout on 45nm technology which is also latest and modern technology in industry perspective. The layout is done by credence tool.

Here 16 N-MOS are present where each and every N-MOS have a common drain which is connected to a single input data bus, so we shared the drain of two N-MOS one over another, in this way we improve our area of the layout also the floor planning is quite easy. Now we used metal-1 to metal-4 for designing our proposed model's layout. At the end it is totally DRC and LVS cleared. The pitch of the layout is 2.5nm as height and 4.5 nm for width which is fixed and optimized minimum area is required [5].



VI. Conclusion

In this paper the barrel shifter is design using pass transistor logic where area is reduced by layout of our proposed model .By using tanner EDA tool 13.2 we simulate our circuit on 22nm,32nm 45nm and 16nm technologies and obtain 45% reduction in power consumption in16 nm technology compared to 22nm.

References

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Sayan Chatterjee has received his B.Tech degree from Pailan College of Management and Technology (West Bengal University of technology) in 2013 and pursuing M.Tech from Heritage Institute of Technology (West Bengal University of Technology). His research interest include embedded system, VLSI architecture and layout designing.