Power Efficient Design of 4 Bit Asynchronous Up Counter Using D Flip Flop

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I. Introduction
Latch is an electronic device which is used to store one bit of data information. When the clock pin at positive edge the output of the D flip-flop takes the state of the D input and delays it by one clock cycle. Hence it is known as delay flip-flop. Latches are used as buffers but flip flops are used as a registers. Flip flop is the basic memory cell which is used to store the value on the data line. It has an advantage that the output is being synchronized by a lock. Many logic synthesis tools use only D latch and D flip flop. The power consumption and area are the main criterion’s considered while designing it. In today’s world power dissipation became a major thing. In today's world power dissipation is the major problem as the high power dissipation leads to reduced time of operation, reduced mobility, high efforts of cooling, operational costs and reduced reliability. As the portable devices needs a good battery life time the low power consumption is needed. In digital systems counter circuits are used for many purposes. The number of occurrences of certain events is counted by using the counters and they generate timing intervals for control of various tasks in a system, keep track of time elapsed between specific events, Frequency synthesizers, frequency dividers and so on. Different types of counters are used in a variety of circuits. Here in this paper a 18 transistor D latch was discussed and from which a 14 transistor D flip flop is proposed and both the designs are compared and an asynchronous up/down counter was designed by using the existing and proposed D flip flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flops and they do not have a global clock like synchronous counter. The proposed and conventional designs are simulated and analyzed in MICROWIND at 1 GHz (90 nm CMOS).

A. Design Approach of Asynchronous Counter Modules
Simply, to operate on n-bit values, we can connect n 1-bit Counters. 4-bit Counter is constructed using four 1-bit register as in our case.

1. Bottom – up- Approach
In a bottom-up approach the individual base elements of the system are first specified in great detail.

II. Implementation of Asynchronous Counter
The counter consists of four stages of cascaded D registers. The D register design has been implemented using CMOS inverter and two D latch with one clock and one input. The clock input is applied to subsequent flip flop comes from the output of its immediately preceding flip flop. For first or instance the output of the first register acts as the clock input to the second register, the output of the second register feed the clock input of third register and the output of the third register feed the clock input of fourth register. The second register can change state only after the output of first register can change its state. That is the second fact that it gets its own clock input from output of the first and not from the input clock. This time delay here the sum of propagation delay of two flip flops. So in this counter four register will change state only after a delay equal to four times the propagation delay of one flip flop.

This is binary counter, since the output is in binary system format, that is only two digits are used to represent the count that is “1” and “0”. With only 4-bits it cans only count up to “1111” or decimal number 15. Counter was designed using 90nm technology. This chapter explains in detail the 4 bit asynchronous counter design.

All of the registers have been implemented using logic gates and then using CMOS logic. Each stage is discussed in detail in the further section of this paper.

A. D Latch
To design a D latch we use universal NAND gates. The D latch is simple gated S R latch with a NAND connected between its S and
Due to inverter S and R is always be the complement of each other. Hence S=R=0 or S = R= 1, these input condition will never appear. And this will avoid the problems associated with SR= 00 and SR = 11 conditions. To design a D latch we saw a working first, with Dsch software that when the clock is low, output is not affected. When the clock is high, the Q output is equals to input D and the notQ output is the inverse of Q.

The previous implementation needs 18 transistors. In order to optimize our design, we decide to use complex gates, which only need 14 transistors. Moreover, we have better propagation delay with its implementation.

### III. Operation of Counter

Now, as we have designed all the components of the counter, we can design it according to the schematic diagram that we have seen in the fig. 5. For each D register we must connect the notQ output to the D input, and the clock signal of each stage (except for the first) is simply carried out by the previous Q output. The first stage receives the clock signal. For the reset, we use the reset of our D registers and we connect them together. However, we need to change the position of the NMOS of the reset of each D register, in order to optimize our layout. Thus, we have not problems with the Q outputs of the counter when we use the reset. Firstly counter is designed by using 90nm technology and simulate with microwind tools.

The following is a 4-bit asynchronous binary counter and its timing diagram for one cycle. It has 16 states due to the fourth flip-flop. This up counter is display 0000 to 1111 binary number, this counter is constructed by using D flip flop as master slave arrangement. The Q1, Q2, Q3 and Q4 are the four states of output of the counter.

Only one flip flop is connected to clock and other flip flops are clocked by previous flip flop’s output. Reset is connected to all the flip flops. When least significant bit makes a transition then information is ripple through all the stats of flip flops. The clock input is applied to subsequent flip flop comes from the output of its immediately preceding flip flop. For instance the output of the first register acts as the clock input to the second register, the output of the second register feeds the clock input of third register and the output of the third register feeds the clock input of fourth register.

As a natural consequence of this all 4 register do not change state at the same time. The second register can change state only after the output of first register can change its state. That is the second fact that it gets its own clock input from the output of the first and not from the input clock. The counter's output is indexed by one LSB every time the counter is clocked. The 4-stage ripple counter displays number from 0 to 15, using a chain of four D-register cell.
Table 1: Comparisons of Asynchronous Counter Using D Flips Flop

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Asynchronous counter using 18T D flips flop</th>
<th>Asynchronous counter using 14T D flips flop</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of transistors</td>
<td>72</td>
<td>56</td>
</tr>
<tr>
<td>Layout Area µm.</td>
<td>43*8</td>
<td>43*13</td>
</tr>
<tr>
<td>Power Consumption µW.</td>
<td>31.06</td>
<td>18.82</td>
</tr>
</tbody>
</table>

V. Conclusion

In this paper we have designed the 18 & 14 Transistor DFF using which the up counter has been designed and simulated in 90nm CMOS technology with MICROWIND tool. From the comparison table1 it is clear that the proposed design has less power consumption in terms of power.

References


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