# Adiabatic Technique for Power Efficient Logic Circuit Design

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**Abstract**
The Power dissipation in conventional CMOS circuits can be minimized through adiabatic technique. By adiabatic technique dissipation in PMOS network can be minimized and some of energy stored at load capacitance can be recycled instead of dissipated as heat. But the adiabatic technique is highly dependent on parameter variation. With the help of MICROWIND simulations, the energy consumption is analyzed by variation of parameter. In analysis, two logic families, ECRL (Efficient Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic) are compared with conventional CMOS logic for inverter NAND and NOR circuits. It is finding that adiabatic technique is good choice for low power application in specified frequency range.

**Keywords**
Power Consumption in CMOS, Adiabatic Technique, Four Phased Power Clock, Equivalent Circuits

## I. Introduction

The term "adiabatic" describe the thermodynamic processes in which no energy exchange with the environment, and therefore no dissipated energy loss. But in VLSI, the electric charge transfer between nodes of a circuit is considered as the process and various techniques can be applied to minimize the energy loss during charge transfer event. Fully adiabatic operation of a circuit is an ideal condition. It may be only achieved with very slow switching speed. In practical cases, energy dissipation with a charge transfer event is composed of an adiabatic component and a non-adiabatic component.

In conventional CMOS logic circuits, from 0 to VDD transition of the output node, the total output energy drawn from power supply and stored in capacitive network. Adiabatic logic circuits reduce the energy dissipation during switching process, and utilize this energy by recycling from the load capacitance. For recycling, the adiabatic circuits use the constant current source power supply and for reduce dissipation it uses the trapezoidal or sinusoidal power supply voltage. The equivalent circuit used to model the conventional CMOS circuits during charging process of the output load capacitance. But here constant voltage source is replaced with the constant current source to charge and discharge the output load capacitance. Hence adiabatic switching technique offers the less energy dissipation in PMOS network and reuses the stored energy in the output load capacitance by reversing the current source. Adiabatic Logic does not abruptly switch from 0 to VDD (and vice versa), but a voltage ramp is used to charge and recover the energy from the output.

Adiabatic circuits are low power circuits which use "reversible logic" to conserve energy.

While this is an area of active research, current techniques rely heavily on transmission gates and four-phased trapezoidal clocks to achieve this goal.

## II. CMOS Logical Families

The types of logic circuits are

- CMOS INVERTER
- CMOS NAND
- CMOS NOR

### A. CMOS Inverter

The most important CMOS gate is the CMOS inverter. It consists of only two transistors, a pair of one N-type and one P-type transistor. As fig.1 shows the basic circuit of CMOS Inverter. Voltage levels are at logical '1' corresponding to electrical level VCC, a logical '0' (corresponding to 0V or GND) .

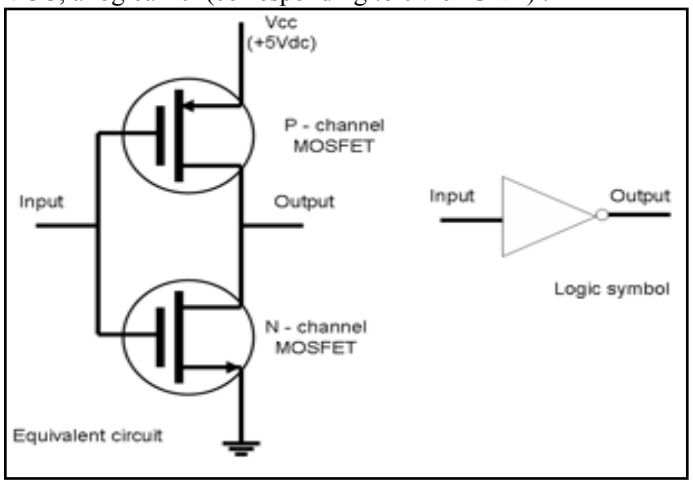


Fig. 1: CMOS Inverter

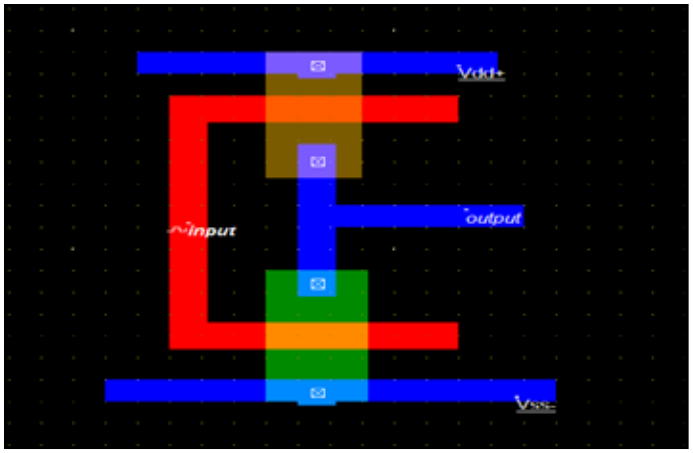


Fig. 2: Layout Design of CMOS Inverter

The layout design of CMOS inverter is drawn according to its circuit diagram as shown in fig. 1. Here, PMOS is in brown color, NMOS is in green color, the metal1 through which they are connected is blue in color. The red color shows polysilicon layer which is used to give input.

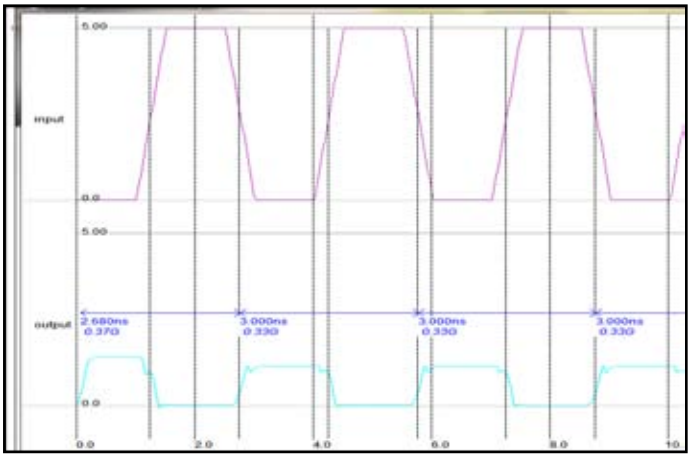

Fig. 3: Simulation Waveform of CMOS Inverter

In this simulation waveform, it is noted that when input is 'High' the corresponding output is 'low'.

CMOS NAND Circuit: A NAND gate (Negated AND or NOT AND) is a logic gate which produces an output that is false only if all its inputs are true. A LOW (0) output results only if both the inputs to the gate are HIGH (1); if one or both inputs are LOW (0), a HIGH (1) output results. The NAND gate is significant because any Boolean function can be implemented by using a combination of NAND gates. This property is called functional completeness.

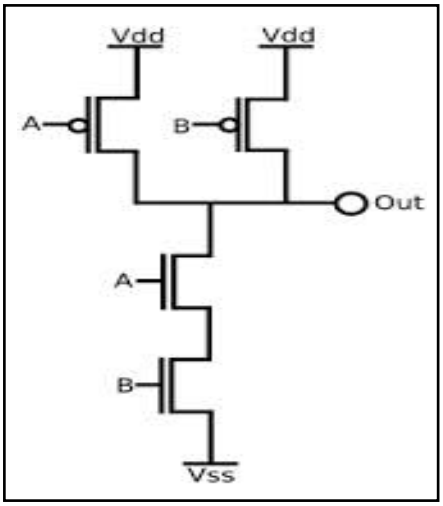

Fig. 4: CMOS NAND Gate Circuit

In CMOS NAND circuit, PMOS are connected in parallel and NMOS is connected in series.

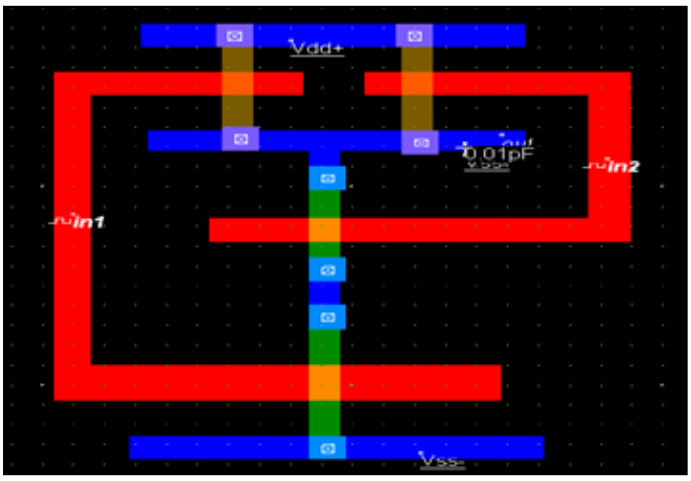

Fig. 5: Layout of CMOS NAND Gate

The layout design of CMOS NAND is drawn according to its circuit diagram as shown in Fig.4. In the two-input NAND gate the P-type transistors are connected in parallel between VCC and the output, while the N-type transistors are connected in series from Vss to the output .

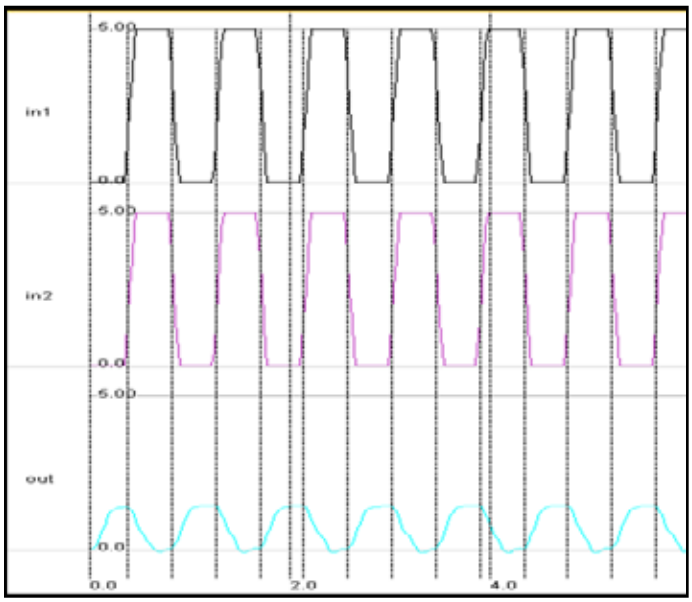

Fig. 6: Simulation Waveform of CMOS NAND Gate

In the simulation waveform, it is seen that when both inputs are at 'High', the corresponding output is 'Low' and vice versa.

### B. CMOS NOR Circuit

The NOR gate is a digital logic gate that implements logical NOR - it behaves according to the truth table to the right. A HIGH output (1) results if both the inputs to the gate are LOW (0); if one or both input is HIGH (1), a LOW output (0) results. NOR is the result of the negation of the OR operator. It can also be seen as an AND gate with all the inputs inverted. NOR is a functionally complete operation—combinations of NOR gates can be combined to generate any other logical function. By contrast, the OR operator is monotonic as it can only change LOW to HIGH but not vice versa.

The layout design of CMOS NOR is drawn according to its circuit diagram as shown in fig. 7. In the two-input NOR gate the P-type transistors are connected in series between VCC and the output, while the N-type transistors are connected in parallel from GND to the output Y.

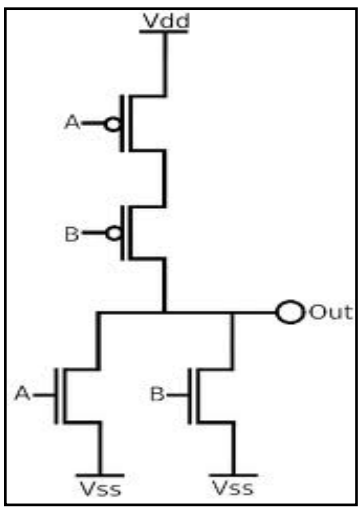

Fig. 7: Circuit of CMOS NOR Gate

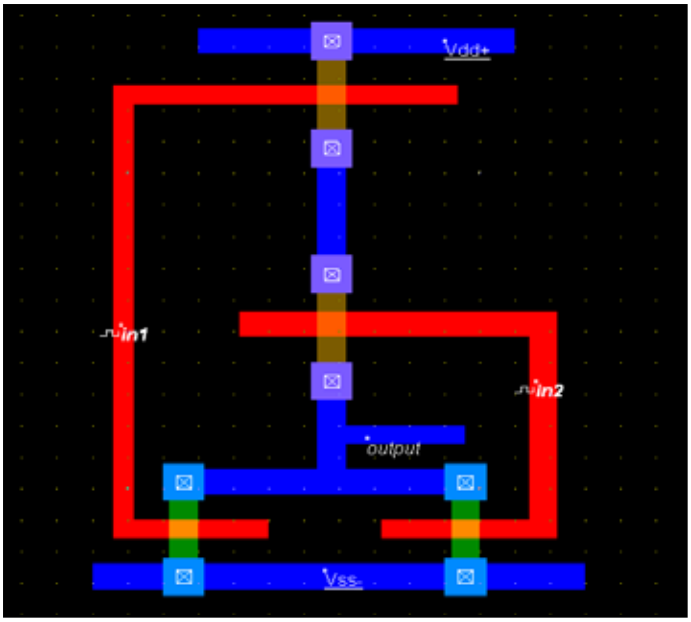


Fig. 8: Layout Design of CMOS NOR Gate

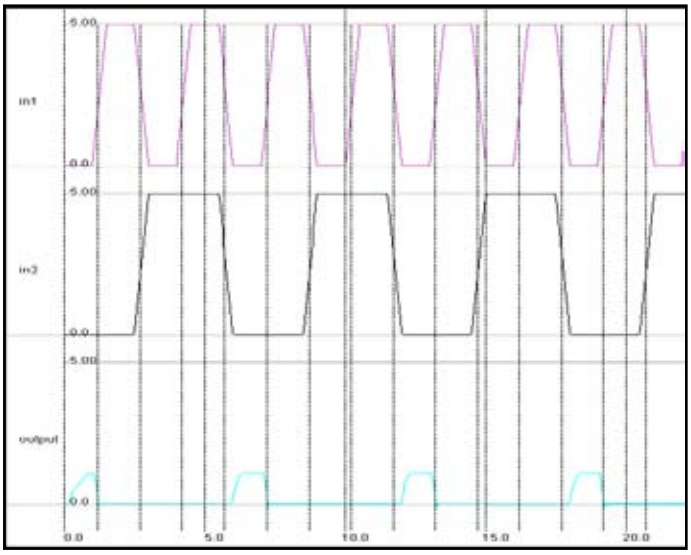


Fig. 9: Simulation Waveform of CMOS NOR Gate

In the simulation waveform, it is seen that when both inputs are at 'Low', the corresponding output is 'High' and vice versa.

## III. Adiabatic Logic Families

We use two types of adiabatic logic circuits ECRL and PFAL for comparative study.

### A. ECRL

Efficient Charge Recovery Logic (ECRL) is proposed as a candidate for low-energy adiabatic logic circuit. Power comparison with other logic circuits is performed on an inverter chain. It adopts a new method that performs pre-charge and evaluation simultaneously. ECRL eliminates the pre-charge diode and dissipates less energy than other adiabatic circuits. An ECRL inverter chain and a pipelined Carry Look Ahead Adder (CLA) are constructed to show the effectiveness of this approach.

### 1. ECRL Inverter

In ECRL inverter, two inverter are cross- coupled to each other and one inverter's input is other's output and vice versa. The ECRL inverter works same as that of basic operation of ECRL.

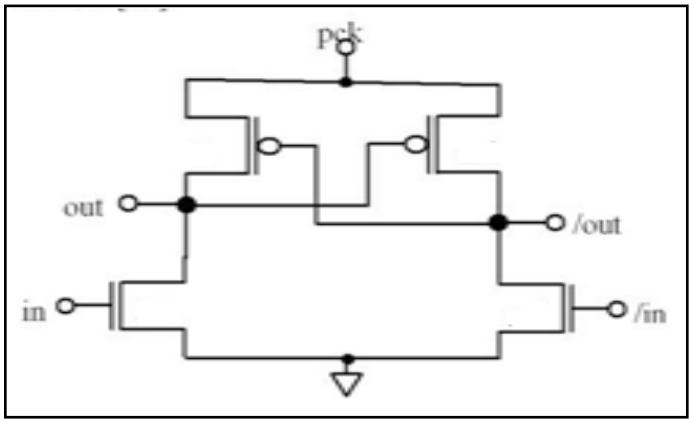


Fig. 10: ECRL Inverter Circuit

The layout design of ECRL inverter is drawn according to its circuit diagram as shown in fig. 10.
The schematic and simulated waveform of the ECRL inverter gate is shown in fig. 10 respectively. Initially, input 'in' is high and input '/in' is low.

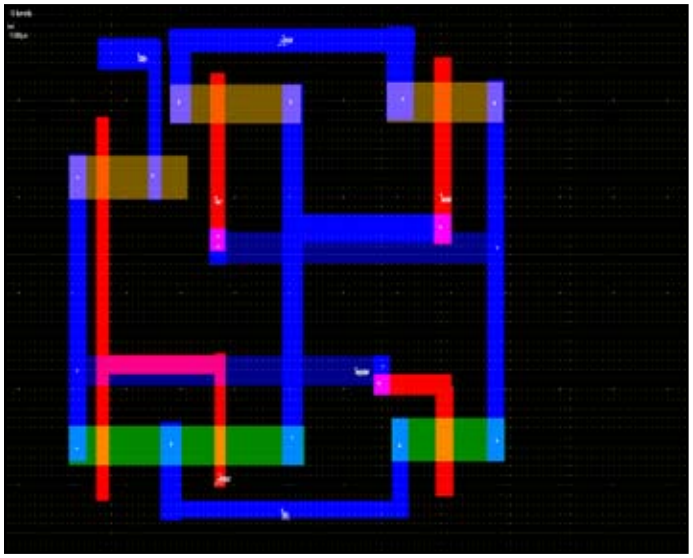

Fig. 11: Layout of ECRL Inverter

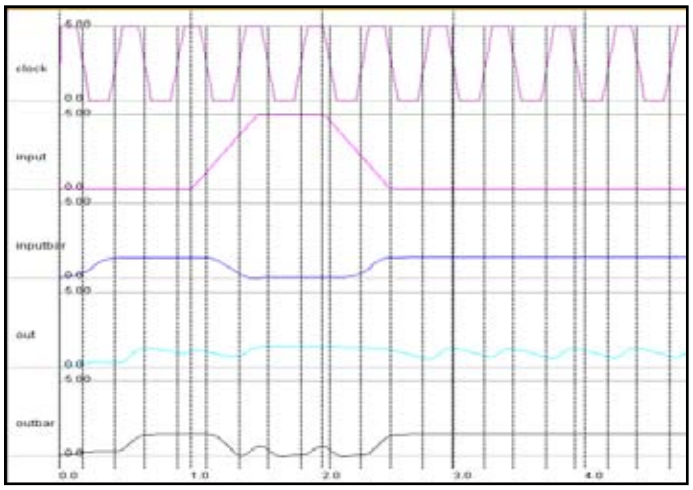


Fig. 12: Simulation Graph of ECRL Inverter

When power clock (pck) rises from zero to VDD, output 'out' remains ground level. Output '/out' follows the pck. When pck reaches at VDD, outputs 'out' and '/out' hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now pck falls from VDD to zero, '/out'

returns its energy to pck hence delivered charge is recovered. ECRL uses four phase clocking rule to efficiently recover the charge delivered by pck.

## 2. ECRL NAND Circuit

The figure shown above is ECRL NAND. It functions same as that of CMOS NAND circuit.

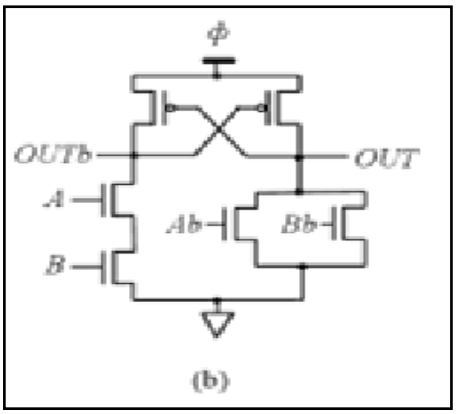


Fig. 13: ECRL NAND Circuit

The layout design of ECRL NAND is drawn according to its circuit diagram as shown in fig. 13.
According to the graph when both inputs are low then output is high and when both the inputs are high then output is low. When one input is high and the other is low then the output is one and vice versa.

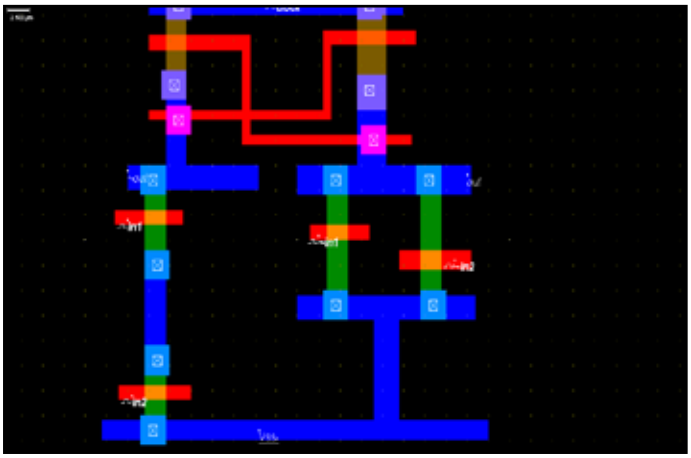

Fig. 14: Layout of ECRL NAND

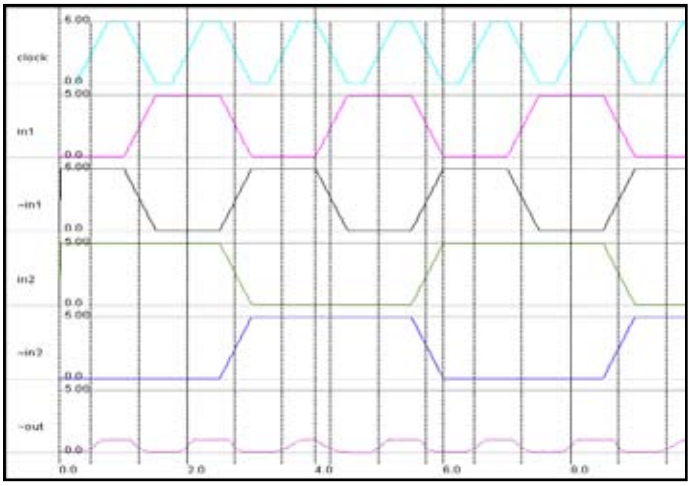


Fig. 15: Simulation Graph of ECRL NAND

## 3. ECRL NOR Circuit

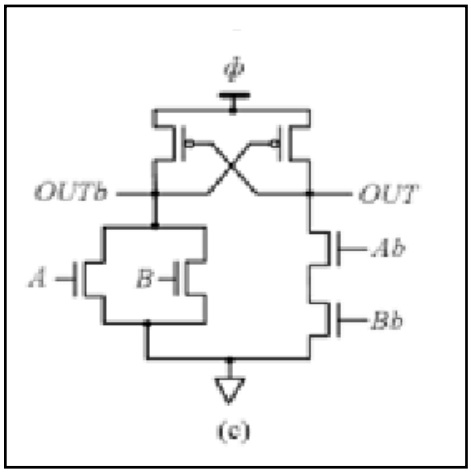


Fig. 16: ECRL NOR Circuit

The fig. 16 shows ECRL NOR circuit functions same as that of CMOS NOR circuit.
The layout design has been drawn in microwind according to the above circuit shown in fig. 16.
According to the waveform when both the inputs are high then the output is low. After that when both the inputs are low then the output is high. If one input is high and the other is low then the output is zero or vice versa.

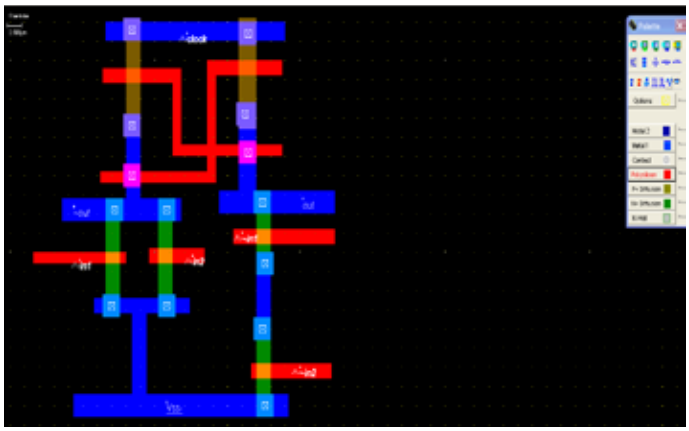

Fig. 17: Layout of ECRL NOR

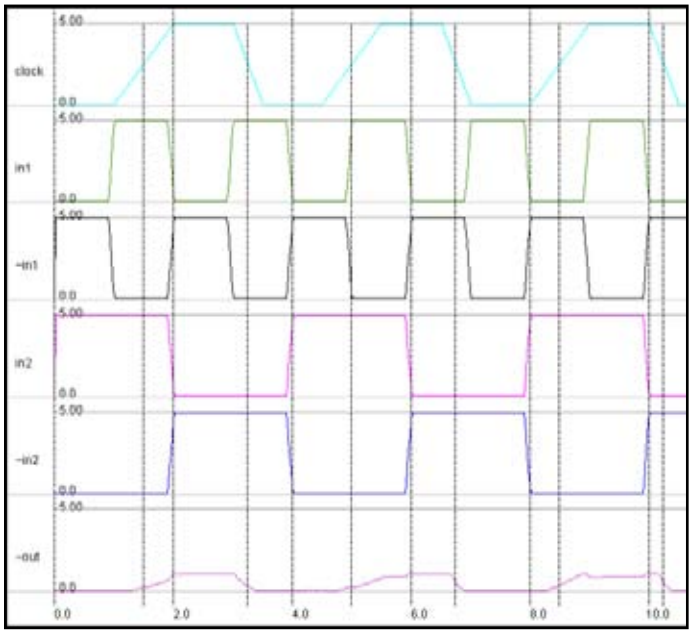


Fig. 18: Simulation Waveform of ECRL NOR

### B. PFAL

The schematic and of the PFAL inverter gate is shown below in Fig 19. Initially, input 'in' is high and input '/in' is low. When power clock (pck) rises from zero to VDD, output 'out' remains ground level. Output '/out' follows the pck. When pck reaches at VDD, outputs 'out' and '/out' hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now pck falls from VDD to zero, '/out' returns its energy to pck hence delivered charge is recovered. PFAL uses four phase clocking rule to efficiently recover the charge delivered by pck.

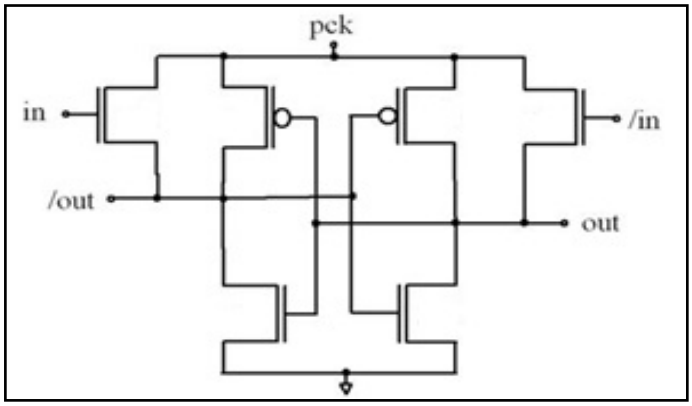


Fig. 19: PFAL Inverter Circuit

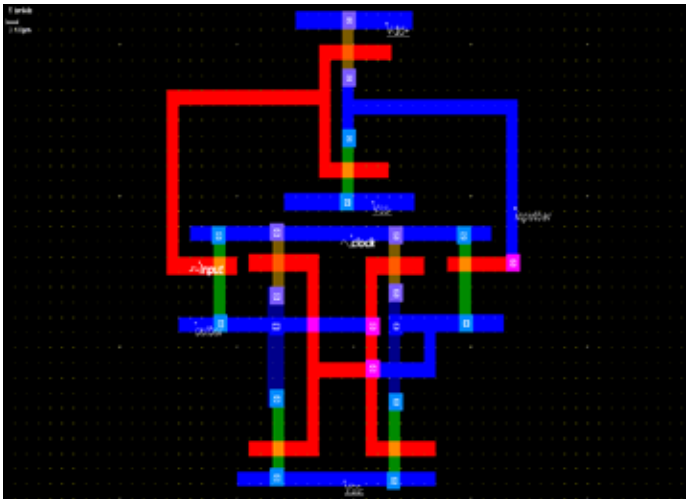

Fig. 20: Layout of PFAL Inverter

The layout design of CMOS inverter is drawn according to its circuit diagram as shown in fig. 19. This simulation waveform shows that when input is 'High', output bar follows the power clock and when input is 'low', the output follows the power clock.

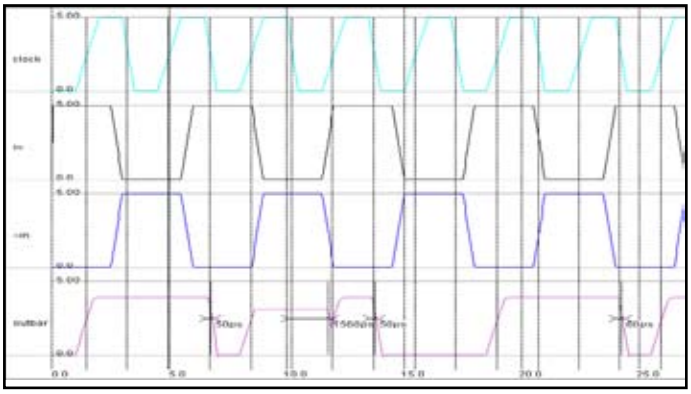

Fig. 21: Simulation Waveform of PFAL Inverter

### A. PFAL NAND Circuit

The fig. 22 is PFAL NAND. It consist of two inverters in which both out and /out are cross coupled to both the inverters. In left side of the inverter two NMOS are connected parallel and in right hand side two NMOS are connected serially. It has power clock and ground connection.

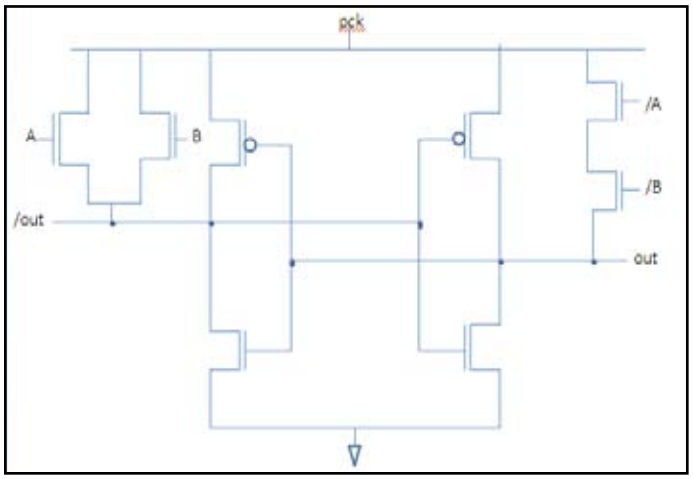


Fig. 22: PFAL NAND Circuit Diagram

The above layout has been design according to the circuit drawn in fig. 22.

According to the graph when both inputs are low then output is high and when both the inputs are high then output is low. When one input is high and the other is low then the output is one and vice versa.

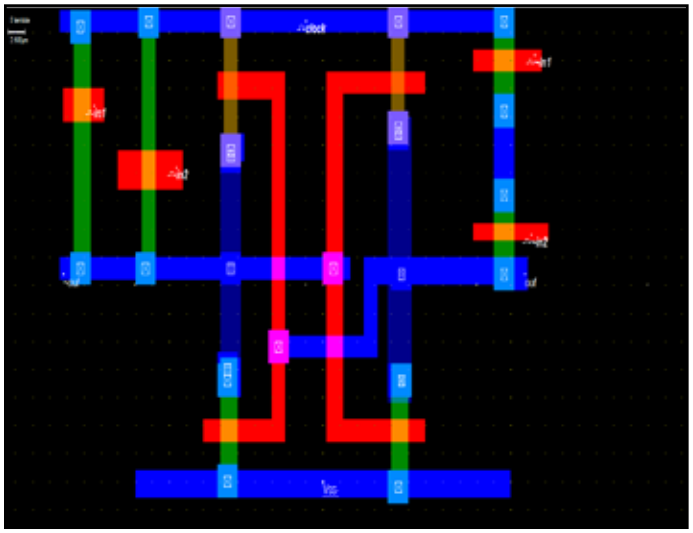

Fig. 23 Layout of PFAL NAND

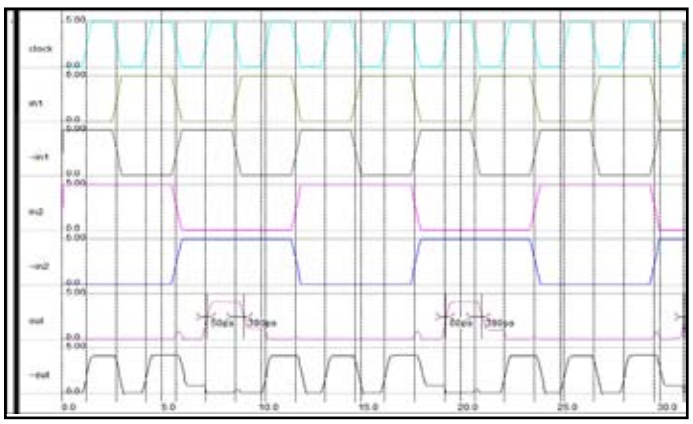

Fig. 24: Simulation Waveform of PFAL NAND

### B. PFAL Nor Circuit

In PFAL NOR circuit two inverters are used and /out and out are cross coupled in the left hand side of the inverter two NMOS are serially connected and in the right hand side of the inverter two NMOS are parallel connected.

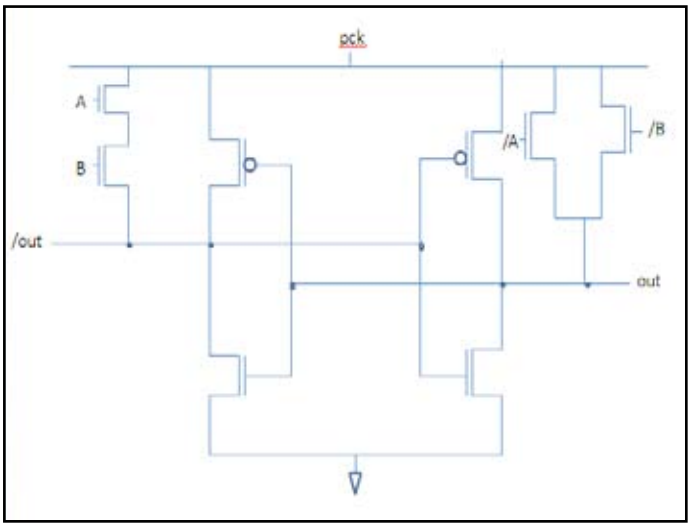


Fig. 25: PFAL NOR Circuit

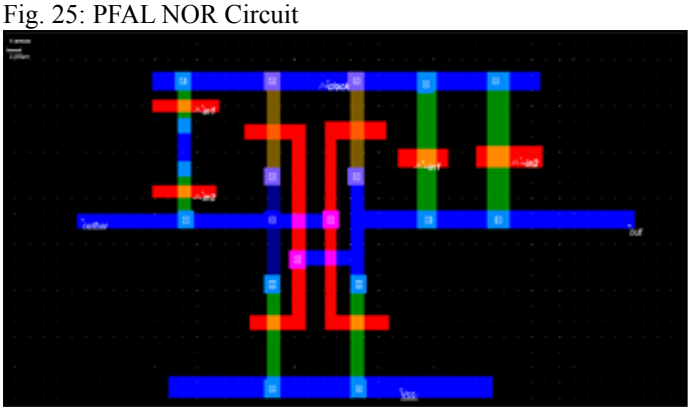

Fig. 26: Layout of PFAL NOR

The layout design has been drawn in micro wind according to the above circuit shown in fig. 25.

According to the waveform when both the inputs are high then the output is low. After that when both the inputs are low then the output is high. If one input is high and the other is low then the output is zero or vice versa.

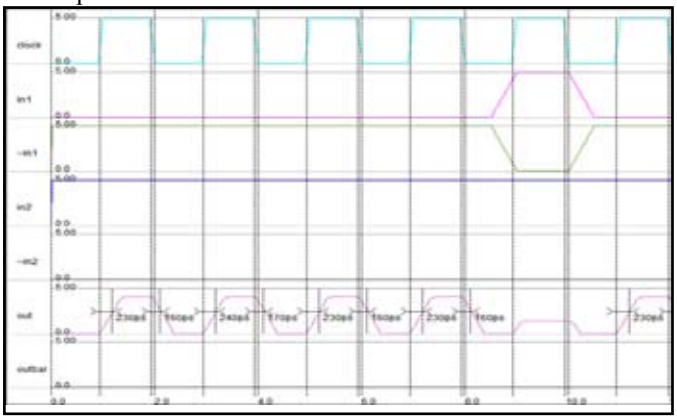

Fig. 27: Simulation Waveform of PFAL NOR

## IV. Power Consumption Coparision and Verification

Following are the parameters on which the power consumption of circuits are to be compared:

- Transition Frequency Variation
- Load Capacitance Variation
- Supply Voltage Variation

### A. Transition Frequency Variation

Fig. 28 shows the power dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the inverter logic. Fig. 29 shows the power dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the NAND logic. Fig. 30 shows the power dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the NOR logic. It is seen that for high frequency the behavior is no more adiabatic and therefore the power dissipation increases. At low frequencies the dissipation energy will increase for both CMOS and adiabatic logic due to the leakage currents of the transistors. During frequency variation Vdd and load capacitance are made constant at certain level. Following are the readings observed by variation of frequency parameters.

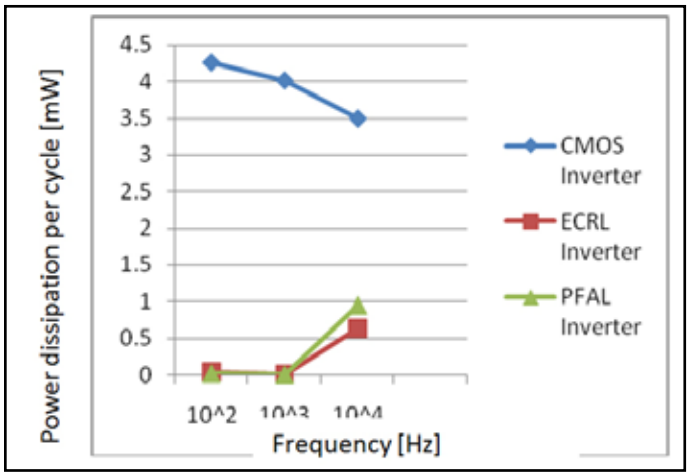


Fig. 28: Power Consumption Per Cycle Versus Frequency for an Inverter at $V_{dd}$=5V and Load Capacitance=5pf.

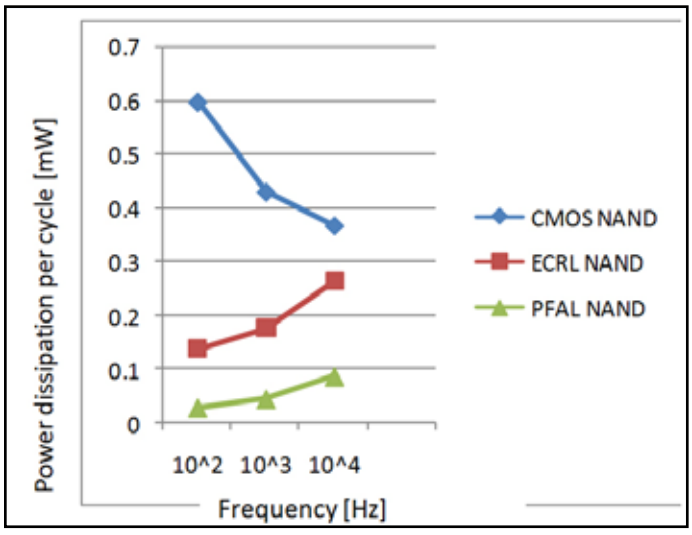


Fig. 29: Power Consumption Per Cycle Versus Frequency for an NAND Logic at $V_{dd}$=5V and Load Capacitance=5pf.

### B. Load Capacitance Variation

Fig. 31 shows the power dissipation per cycle versus load capacitance of the two adiabatic logic families and CMOS for the inverter logic. Fig. 32 shows the power dissipation per cycle versus load capacitance of the two adiabatic logic families and CMOS for the NAND logic. Fig. 33 shows the power dissipation per cycle versus load capacitance of the two adiabatic logic families and CMOS for the NOR logic.

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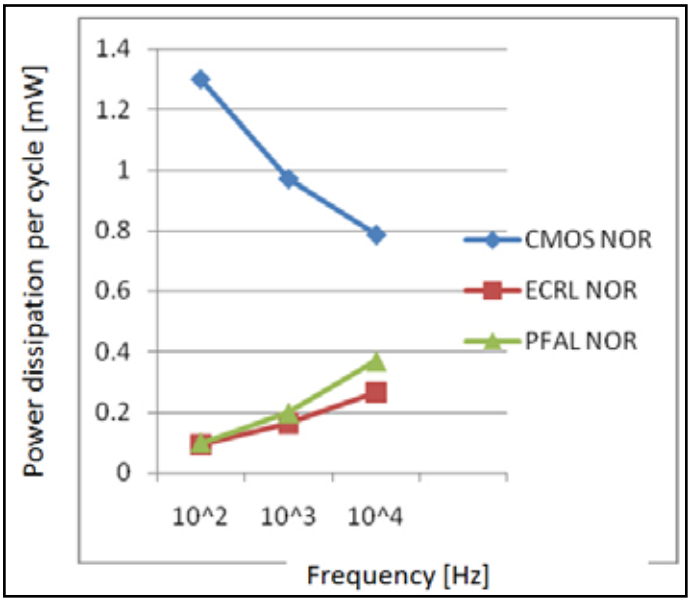


Fig. 30: Power Consumption Per Cycle Versus Frequency for an NOR Logic at $V_{dd}$=5V and Load Capacitance=5pf.

The Figures show that adiabatic logic families having better energy savings than CMOS logic over wide range of load capacitances. PFAL shows better energy shavings than ECRL at high load capacitance.

During Load Capacitance variation, $V_{dd}$ and Frequency are made constant at certain value. Following are the readings observed by variation of Load Capacitance parameters.

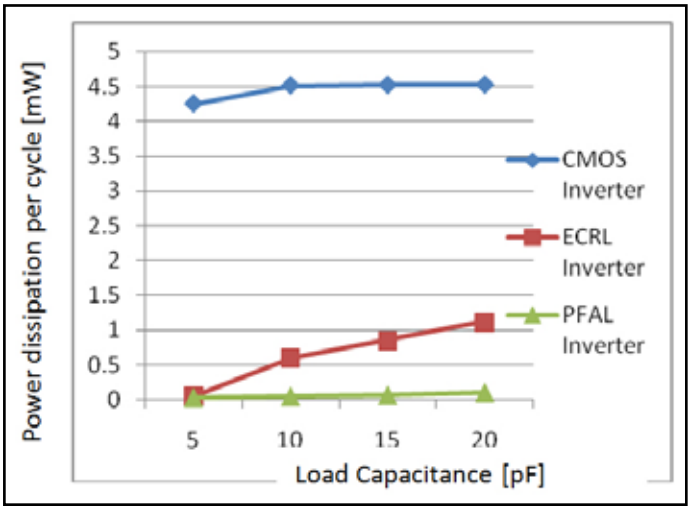


Fig. 31: Power Consumption Per Cycle Versus Load Capacitance for an Inverter at $V_{dd}$=5V and Frequency=100 MHz

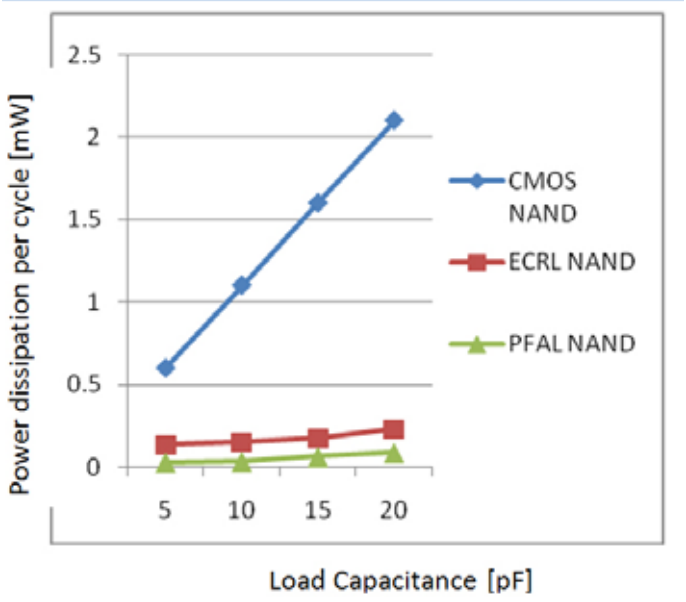


Fig. 32: Power Consumption Per Cycle Versus Load Capacittance for an NAND Logic at $V_{dd}$=5V and Frequency=100 MHz.

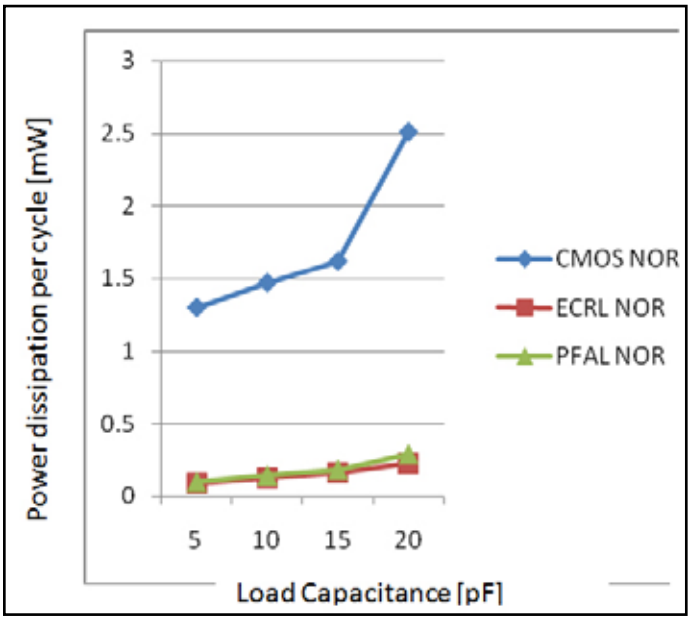


Fig. 33: Power Consumption Per Cycle Versus Load Capacittance for an NOR Logic at $V_{dd}$=5V and Frequency=100 MHz.

### C. Supply Voltage Variation

Fig. 34 shows the power dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the inverter logic. Fig. 35 shows the power dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the NAND logic. Fig. 36 shows the power dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the NOR logic. It is seen that supply voltage decreases, the gap between CMOS and logic families is reduced. But ECRL and PFAL still shows large energy savings over wide range of supply voltage. During Supply Voltage variation, Frequency and Load Capacitance are made constant at certain value.

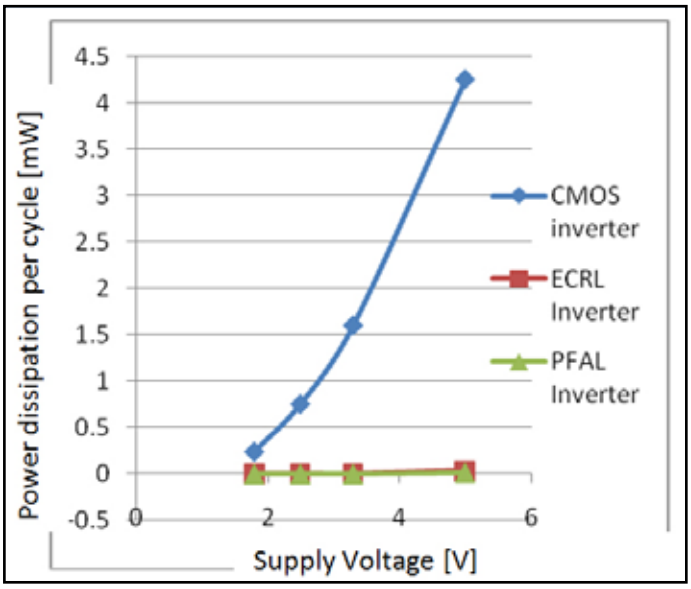


Fig. 34: Power Consumption Per Cycle Versus Supply Voltage for an Inverter at Load Capacitance=5pF and Frequency=100 MHz

Following graph has been made with respect to the corresponding observation.

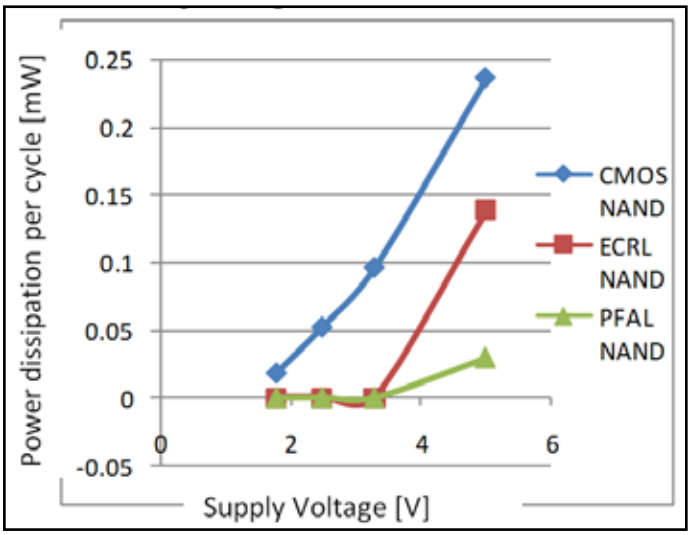


Fig. 35: Power Consumption Per Cycle Versus Supply Voltage for an NAND Logic at Load Capacitance=5pF and Frequency=100 MHz.

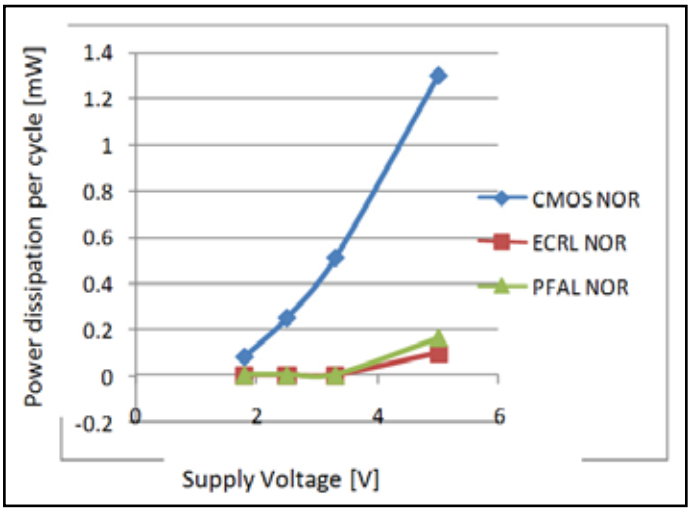


Fig. 36: Power Consumption Per Cycle Versus Supply Voltage for an NOR Logic at Load Capacitance=5pF and Frequency=100 MHz

## VI. Conclusion

The different parameter variations against adiabatic logic families are investigated, which shows that adiabatic logic families highly depend upon its parameter variations. But less energy consumption in adiabatic logic families can be still achieved than CMOS logic over the wide range of parameter variations. PFAL shows better energy shavings than ECRL at the high frequency and high load capacitance. Specially PFAL NOR has better Efficiency of power saving among all the circuits. Hence adiabatic logic families can be used for low power application over the wide range of parameter variations.

ECRL is a low-energy, adiabatic logic. Simulation indicates power saving over static and other adiabatic logic families. The ECRL inverter chain shows 10-20 times power gain over a conventional inverter chain. ECRL shows large power saving and shows the promising usage of ECRL in a low power system.

PFAL has the potential to be used to implement arbitrary reversible logic functions. It has also been shown that by making PFAL fully reversible, considerably reduced power consumption can be obtained.

With the adiabatic switching approach, circuit energies are conserved rather than dissipated as heat. Depending on the application and the system requirements, this approach can sometimes be used to reduce the power dissipation of digital systems.

## VII. Future Work

- In future, more adiabatic logic are to be introduced which can help in overcoming the disadvantages of recent adiabatic logic circuits. For example- DFAL (Diode Free Adiabatic Logic Circuit).
- Research in going on in introducing carbon nanotube based adiabatic logic. If carbon annotates become successors to planar CMOS transistors they offer a tremendous energy saving impact and improved performance especially in Adiabatic Logic. Due to their superior carrier transport they offer a small on-resistance and thus are exceptionally well applicable in Adiabatic Logic, where energy per operation depends not only on capacitance, as in static CMOS, but also on resistance.
- Study of comparison of adiabatic logic connected with different types of multipliers in different parameters may also be done in future.
- Future work also includes the design of larger adiabatic gates and circuits from the proposed buffer/inverter and dissipated energy analysis at higher frequencies and comparison with other adiabatic families.

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