

An Efficient Embedded DRAM Testing Algorithm With Multiple Memory Arrays

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Abstract

With the strong need to an effective and economic embedded-memory core in the Soc, researchers attempt to carry commodity DRAM's advantages from a commodity memory into a Soc. In the past decade, a lot research effort has been put into the area of the embedded-DRAM (eDRAM) technologies to reduce eDRAM's process adders to the CMOS process. However, few previous research works have discussed the testing strategies used for eDRAMs, which cannot be directly carried from the testing of commodity DRAMs. In this project, first compare the eDRAM testing to the commodity-DRAM testing and SRAM testing since an eDRAM core utilizes the DRAM cells with the SRAM interface. Then, list the fault models which should be specially considered in the eDRAM testing and find out the corresponding test sequence for each fault model. The main objectives of this project include (1) develop a minimal test algorithm for eDRAM testing, (2) develop an effective scheme to shorten the retention-test time in eDRAM testing based on increasing the temperature, which is a special function used in eDRAMs compared to commodity DRAMs.

Keywords

Embedded-DRAM (eDRAM), Fault Model, Retention Test Time

I. Introduction

DUE to the advantages of high density, structure simplicity, low-power consumption, and low cost, DRAM has been the mainstream of the commodity-memory market since its invention by Dr. Dennard [1]. With the continually growing need to an effective and economic embedded-memory core in the SoC era, researchers attempt to carry DRAM's advantages from a commodity memory into a SoC. In the past decade, a lot research effort has been put into the embedded-DRAM (eDRAM) technologies, such as deep-trench capacitors with bottle etch to reduce the process adders to the CMOS process, where the eDRAM is embedded in. The eDRAM technologies are now available in the IC-foundry industry [6], [7] and its applications include the products of networking, multimedia handheld devices, gaming consoles, high definition television, and so forth.

Unlike integrating a bare DRAM die within a system-in-package or a packaged DRAM on a system board, where the responsibility of testing the commodity DRAM itself is on the memory design company, the responsibility of testing the eDRAM is transferred to the system integrator. Testing large embedded-memory cores has been a big challenge for SoC testing due to the difficulty of test isolation and test accessibility [8]. By reducing the tester requirement and enabling the parallel testing of different memory cores, memory built-in-self-test (BIST) circuit is the best solution to the embedded memory testing in common consensus today [9]. Several BIST schemes are proposed for the embedded DRAM testing. However, these previous works mainly focus on the architecture and the automatic generation of the BIST circuitry. Few discussions on the test algorithms and the test-time overhead resulted from the retention test can be found in the literature for the eDRAM testing.

In fact, testing eDRAMs is quite different from testing commodity DRAMs due to the following reasons. First of all, most eDRAM macros use the SRAM interface (the so-called 1T-SRAM architecture), which consists of no address multiplexer (no CAS, RAS) and can auto-refresh. Second, unlike commodity DRAM, whose application might be unknown before the fabrication, eDRAM macros are more application-specific and hence have only one operating mode, meaning that one cycle latency at only one operating frequency needs to be tested. Due to the use of a simple SRAM interface in eDRAMs, testing eDRAMs is more like testing SRAMs and requires a shorter test algorithm than testing commodity DRAMs. However, testing eDRAM is not as simple as testing SRAMs since some fault models which may not occur in SRAMs, such as retention faults and coupling faults, may occur in eDRAM.

Similar to commodity DRAMs, eDRAMs require a retention test as well. The specification of eDRAM's data-retention time is a constant and usually in the order of milliseconds. As a result, the ratio of this retention test time over the eDRAM test time increases when the clock frequency of the eDRAM increases. It implies that the retention-test time may dominate the eDRAM test time for high-performance eDRAM designs. The data-retention time of an eDRAM cell depends on the leakage current of the switch transistor in the cell, which is sensitive to the temperature.

The remainder of this paper is organized as follows. Section II first introduces the embedded DRAM architecture in use. Section III presents a reduced, effective test algorithm for eDRAMs. Section IV discusses the leakage mechanism of a switch transistor and analyzes the retention-test time at different temperatures. The conclusion is given in Section V.

II. Overview of Embedded DRAM

Fig. 1 shows the block diagram of a 16 Mb eDRAM macro used in our SoC design. This eDRAM macro utilizes deep trench capacitors and is implemented in a UMC 65 nm low-leakage logic process. Fig. 2 shows a cross-section view of an eDRAM cell in our design. The word size on the interface of this eDRAM macro is 32 bits. Due to the use of ECC, we need to add 6-bit more memory cells to the physical array for each word, and hence the physical data stored in the memory array is 38 bits per word. A physical 38-bit word is read out from or written into the memory array through the ECC circuitry, which encodes a 32-bit word into a 38-bit word or decodes a 38-bit word to a 32-bit word. The size of the eDRAM macro is around 4 mm, which contains two symmetric eDRAM arrays. Each array contains 128 banks, and each bank contains 64 word-lines and its own local sense amplifier.

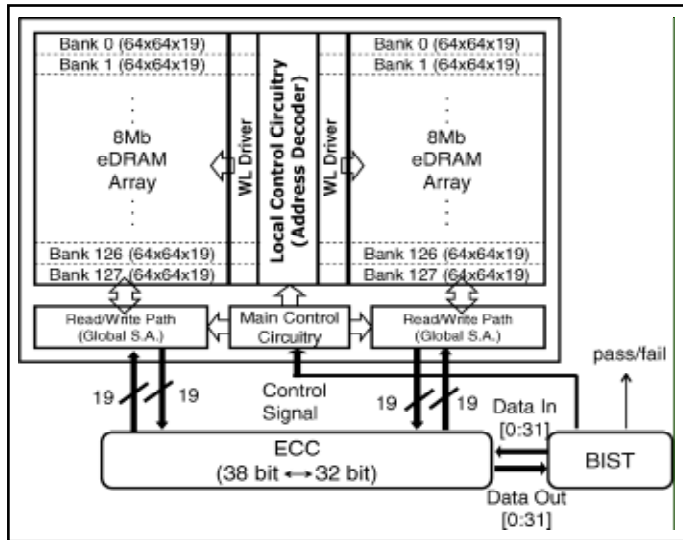


Fig. 1: E-DRAM Architecture

Note that the layout topology of the eDRAM array utilizes the distributed folding scheme, where the i th bit of the j th word is adjacent to the i th bit of the $(j+1)$ th word, not the $(i+1)$ th bit of the original j th word. Between the two eDRAM arrays is the address decoder including word-line drivers. The control circuit (CTL) and Global Sense Amplifier (GSA) are on the bottom of the eDRAM core.

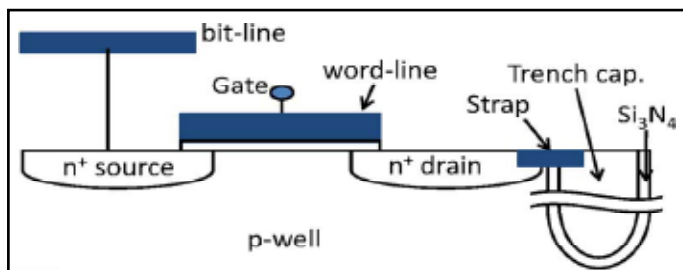


Fig. 3: Illustration of an eDRAM Cell

III. EDRAM Test Approach

A. Current SRAM Test Approach

In this section, we use the March C- algorithm as the basic skeleton of our eDRAM-testing algorithm. March C- algorithm is currently the most widely used test algorithm for SRAM in industry, which can detect Stuck-At Faults (SAFs), Transition Faults (TFs), address decoder faults (AFs), inversion coupling faults (CFins), idempotent coupling faults (CFids), and state coupling faults (CFst) [1]. The following shows the element sequence of the March C- algorithm. The complexity of the March C- algorithm is $10N$, where N is the density of the array.

March C- ($10N$):

$$\{\uparrow (wa); \uparrow (ra, wb); \uparrow (rb, wa); \downarrow (ra, wb); \downarrow (rb, wa); \uparrow (ra)\}$$

B. Proposed Embedded-DRAM Test Approach

This test approach applies an X-direction extended March C- algorithm with solid data-background as well as a Y-direction MATS algorithm with checkerboard data-background. Also, we test the self-refresh operation in the extended March C algorithm and the retention faults in the MATS algorithm. The auto-refresh

is always on in both algorithms. The detail steps of the March C- and MATS algorithms are described as follows.

X-direction Extended March C- with solid background:

$$\text{EMC-: } \{\uparrow (wa); \uparrow (ra, wb, rb); (SR); \uparrow (rb, wa); \downarrow (ra, wb); \downarrow (rb, wa); (SR); \uparrow (ra)\}.$$

Y-direction MATS with checkerboard background:

$$\text{MATS: } \{\uparrow (wa); SR; del; \uparrow (ra, wb); SR; del; \downarrow (rb)\}.$$

SR self-refresh; Del delay element which stops for the period of the retention time defined in the specification.

The test time (in terms of cycles) of the above EMC- and MATS algorithms are listed in (1) and (2)

$$\text{EMC-} : 11N + 2 \times \frac{N}{64} \quad (1)$$

$$\text{MATS} : 4N + 2 \times \frac{N}{64} + 2 \times T_R \times f \quad (2)$$

The above X-direction extended March C- algorithm covers the stuck-open faults by the element (ra, wb, rb) . It also tests the functionality of self-refresh and auto-refresh. The above Y-direction MATS algorithm tests the word-line-coupling faults by the Y-direction elements and checkerboard data-background. It also tests the retention faults by inserting the sequence of SR and del twice. The bit-line-toggling faults are covered by the solid background operations in the extended March C- algorithm.

C. Test Time Analysis for Proposed Test Approach

The total test time of the proposed test approach is the summation of the test time on retention test, read/write operations, self-refresh, and auto-refresh is equal to the retention-time specification, and is equal to the runtime divide by the specified retention time.

$$T_{\text{test}} = T_{RT} + T_{R/W} + T_{SR} + T_{AR} \quad (3)$$

$$T_{RT} = 2 \times T_{del} \quad (4)$$

$$T_{R/W} = N_{\text{WORDS}} \times N_{R/W} \times T_{\text{CYCLE}} \quad (5)$$

$$T_{SR} = N_{WL} \times N_{SR} \times T_{\text{CYCLE}} \quad (6)$$

$$T_{AR} = N_{WL} \times N_{AR} \times T_{\text{CYCLE}} \quad (7)$$

Table 1 lists the test time spent in each component of the proposed approach, given a 50 MHz clock frequency and a 16ms retention-time specification. In this case, the ratio of retention-test time to total test time is 17.4%.

Table 1: Test Time Distribution of the Proposed Test Approach

	retention	read & write	self-refresh	auto-refresh	total	retention ratio
test time (ms)	32	150	0.6	1.3	183.9	17.4%

In current eDRAM designs, the target clock frequency can be higher than the 50 MHz used in Table 1. Table 2 shows the ratio of the retention-test time to total eDRAM-test time for different clock frequencies and different retention-time specifications. As the results show, the ratio of the retention-test time increases when the clock frequency increases, and gradually dominates the total

eDRAM-test time. If the retention time is defined longer in the specification, this ratio would be even higher. For the case that clock frequency is 200 MHz and the defined retention time is 32 ms, this retention-test-time ratio can be up to 62.9%.

Table 2: Ratio of Retention-Test Time to Total Test Time w.r.t. each Retention-Time Specification and Clock Rate

retention time in spec. (ms)	retention test time (ms)	clock rate (MHz)	total test time (ms)	ratio of retention-test time to total test time
16	32	50	183.9	17.4%
		100	107.5	29.8%
		200	69.7	45.9%
32	64	50	214.9	29.8%
		100	139.3	45.9%
		200	101.7	62.9%

IV. Reducing Retention-Test Time by Increasing Temperature

For an eDRAM cell, its data-retention time is determined by the leakage of its switch transistor, which increases along with the increase of the temperature. In the eDRAM testing, we attempt to raise the temperature to increase transistor's leakage current, which shortens the data-retention time of a cell.

Therefore, at a higher temperature, the delay element used for retention test can be specified shorter since a retention fault can be detected within a shorter period of time than that at the original reference temperature. However, if the new specified retention time is too low, some retention faults may be able to escape, resulting in a higher defect level. On the contrary, if it is too high, the retention time of an eDRAM cell is over-tested, resulting in a yield lost.

A. Analysis of Equivalent Retention Time

To calculate the equivalent retention time for a target temperature, we first calculate the total amount of charge leaked from the storage capacitor during the retention-time specification at the reference temperature, i.e., 850C. Then the leakage during the equivalent retention time at the target temperature has to be equivalent to, which is expressed in (8)

$$Q_{\text{total}} = I_{\text{leak}}(\theta_{\text{ref}}) \times T_{\text{ref}} = I_{\text{leak}}(\theta_{\text{tat}}) \times T_{\text{eqv}} \quad (8)$$

Therefore, the equivalent retention time at the target temperature can be obtained by (9)

$$T_{\text{eqv}} = \frac{I_{\text{leak}}(\theta_{\text{ref}}) \times T_{\text{ref}}}{I_{\text{leak}}(\theta_{\text{tat}})} \quad (9)$$

Table 3 lists the calculated equivalent retention time and its reduction ratio to the original specification-defined retention time associated with each given temperature. The retention-time specification is 16 ms at the reference temperature 850C. As the results shows, the retention-time reduction is close to 50% when raising the temperature to 105 0C, and 65% when 1200C, respectively. It implies that the retention-test time can be significantly reduced by raising the temperature.

Table 3: Calculated Equivalent Retention Time and its Reduction to the Retention-Time Specification 16 ms at 850C

D. Experimental Results With ECC-Off

In this subsection, we would like to share some internal experimental results which helped us to design the March elements, traversing direction, and data background used in our proposed test approach during the development stage. Those experiments are conducted by applying several similar march algorithms to the same eDRAM macros and comparing their resulting yields.

Table 3: Test Algorithm of A1, A2, AND A3

March Algorithm	March Operations	Data Background	Traversing Direction
A1	MATS	Checkerboard	Y
A2	MATS		X
A3	{↑(wa,ra),↓(wb,rb)}		X

Table 3, lists the March elements, data background, and traversing direction of three 4N March algorithms, denoted as A1, A2, and A3. As Table IV shows, A1 is the Y-direction MATS algorithm with checkerboard background, which is actually the same algorithm used in the first part of our proposed test approach.

Table 4: Test Algorithm of B1 AND B2

March Algorithm	March Operations	Data Background	Traversing Direction
B1	EMC-	Solid	X
B2		Checkerboard	

Table 5: Test Algorithm of C1, C2, AND C3

March Algorithm	March Operations	Data Background	Traversing Direction
C1	MATS	Checkerboard	X
C2	MATS with retention test		
C3	MATS with byte-write test		

Table 4, lists the March elements, data background, and traversing direction of two EMC- algorithms, denoted as B1 and B2. As Table IV shows, B1 uses a solid background while B2 uses a checkerboard background. Both B1 and B2 traverse in X-directional. Table V lists description of three different MATS algorithms, denoted as C1, C2, and C3. C1 is the -direction checkerboard-background MATS algorithm and does not include the retention test (same as A2). C2 is C1 plus retention test. C3 is C1 with all its write operations performed by byte-write, i.e., writing a byte (8) of bit-cells at a time instead of a word (32).

E. Test Time Analysis for Proposed Test Approach

The total test time of the proposed test approach is the summation of the test time on retention test, read/write operations, self-refresh, and auto-refresh is equal to the retention-time specification, and is equal to the runtime divide by the specified retention time.

$$T_{\text{test}} = T_{\text{RT}} + T_{\text{R/W}} + T_{\text{SR}} + T_{\text{AR}} \quad (3)$$

Where

$$T_{\text{RT}} = 2 \times T_{\text{del}} \quad (4)$$

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$$T_{AR} = N_{WL} \times N_{AR} \times T_{CYCLE} \quad (7)$$

Table 6, lists the test time spent in each component of the proposed approach, given a 50 MHz clock frequency and a 16ms retention-time specification. In this case, the ratio of retention-test time to total test time is 17.4%.

Table 6: Test Time Distribution of the Proposed Test Approach

	retention	read & write	self-refresh	auto-refresh	total	retention ratio
test time (ms)	32	150	0.6	1.3	183.9	17.4%

In current eDRAM designs, the target clock frequency can be higher than the 50 MHz used in Table VI. Table VII shows the ratio of the retention-test time to total eDRAM-test time for different clock frequencies and different retention-time specifications. As the results show, the ratio of the retention-test time increases when the clock frequency increases, and gradually dominates the total eDRAM-test time. If the retention time is defined longer in the specification, this ratio would be even higher. For the case that clock frequency is 200 MHz and the defined retention time is 32 ms, this retention-test-time ratio can be up to 62.9%.

Table 7: Ratio of Retention-Test Time to Total Test Time W.R.T. Each Retention-Time Specification and Clock Rate

retention time in spec. (ms)	retention test time (ms)	clock rate (MHz)	total test time (ms)	ratio of retention-test time to total test time
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For an eDRAM cell, its data-retention time is determined by the leakage of its switch transistor, which increases along with the increase of the temperature. In the eDRAM testing, we attempt to raise the temperature to increase transistor's leakage current, which shortens the data-retention time of a cell. Therefore, at a higher temperature, the delay element used for retention test can be specified shorter since a retention fault can be detected within a shorter period of time than that at the original reference temperature. However, if the new specified retention time is too low, some retention faults may be able to escape, resulting in a higher defect level. On the contrary, if it is too high, the retention time of an eDRAM cell is over-tested, resulting in a yield lost.

A. Analysis of Equivalent Retention Time

To calculate the equivalent retention time for a target temperature, we first calculate the total amount of charge leaked from the storage capacitor during the retention-time specification at the reference temperature, i.e., 850C. Then the leakage during the equivalent retention time at the target temperature has to be equivalent to, which is expressed in (8)

$$Q_{\text{total}} = I_{\text{leak}}(\theta_{\text{ref}}) \times T_{\text{ref}} = I_{\text{leak}}(\theta_{\text{tat}}) \times T_{\text{eqv}} \quad (8)$$

Therefore, the equivalent retention time at the target temperature can be obtained by (9)

$$T_{\text{eqv}} = \frac{I_{\text{leak}}(\theta_{\text{ref}}) \times T_{\text{ref}}}{I_{\text{leak}}(\theta_{\text{tat}})} \quad (9)$$

Table VIII lists the calculated equivalent retention time and its reduction ratio to the original specification-defined retention time associated with each given temperature. The retention-time specification is 16 ms at the reference temperature 85°C. As the results shows, the retention-time reduction is close to 50% when raising the temperature to 105 °C, and 65% when 120°C, respectively. It implies that the retention-test time can be significantly reduced by raising the temperature.

Table 3: Calculated Equivalent Retention Time and its Reduction to the Retention-Time Specification 16 ms at 85°C

	90°C	95°C	100°C	105°C	110°C	115°C	120°C
retention time (ms)	13.57	11.55	9.87	8.47	7.29	6.30	5.47
reduction ratio	15.2%	27.8%	38.3%	47.1%	54.4%	60.6%	65.8%

B. Experimental Results

In the following experiment, we apply our proposed test algorithm (described in Section III) on the eDRAM cores of 1-lot test wafers repeatedly with different retention-time specifications at different temperatures. In each time of the eDRAM testing, the delay element needs to match the retention-time specification. Table 4 shows the corresponding yield for each retention-time specification and temperature. As the results show, the yield reaches 86.5% with 16 ms retention time at 85°C. Also, the same yield is first-reached with 12 ms retention time at 95°C and 8 ms retention time at 105°C. This result implies that the eDRAM cells which hold their charge for 16 ms at 850C can hold their charge for 12 ms at 950C and for 8 ms at 1050C, respectively.

Table 4: Yield w.r.t. Each Temperature and Retention-Time Specification

retention time (ms)	85°C	95°C	105°C
16	86.5%	83.1%	77.5%
14	86.5%	84.3%	82.0%
12	86.5%	86.5%	83.1%
10	86.5%	86.5%	83.1%
8	86.5%	86.5%	86.5%
6	86.5%	86.5%	86.5%
4	86.5%	86.5%	86.5%

Table 5 further shows the total eDRAM-test-time reduction which can be achieved by increasing the testing temperature. As the results show, this total eDRAM-test-time reduction increases when the temperature, clock frequency, or retention-time specification increases. The reduction ratio can be up to 38.2% by increasing 300C at temperature when the retention-time specification and clock frequency are 32 ms and 200 MHz, respectively. Note that at a higher temperature, its equivalent retention time decreases, which results in more frequent auto-refresh operations. Fortunately, the

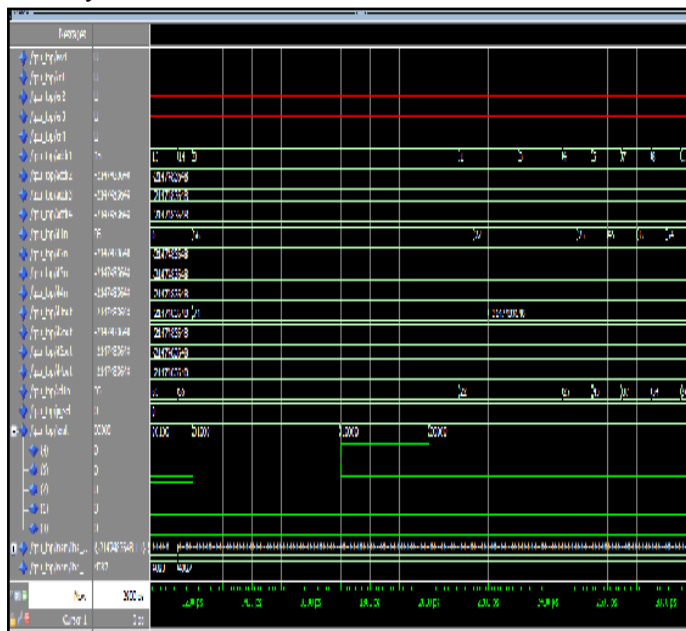
time consumed by a refresh operation is short and does not affect test-time reduction too much. If we want to test the data retention after package, the temperature under consideration should be the temperature inside the package, not just tester's temperature.

Table 5: Test Time Reduction w.r.t. Each Retention-Time Specification, Clock Rate, and Temperature

retention time in spec.	clock rate (MHz)	temp. (°C)	equivalent retention time (ms)	retention test time (ms)	total test time (ms)	test-time reduction to 85°C
16ms	50	85	16	32	183.9	-
		95	11.55	23.1	175.3	4.8%
		105	8.47	16.94	170.2	7.4%
		115	6.3	12.6	167.0	9.2%
	100	85	16	32	107.5	-
		95	11.55	23.1	98.6	8.3%
		105	8.47	16.94	92.8	13.7%
		115	6.3	12.6	88.7	17.5%
	200	85	16	32	69.7	-
		95	11.55	23.1	60.8	12.8%
		105	8.47	16.94	54.6	21.7%
		115	6.3	12.6	50.6	27.4%
32ms	50	85	32	64	214.9	-
		95	23.1	46.2	197.3	8.2%
		105	16.94	33.88	185.8	13.5%
		115	12.61	25.22	177.4	17.4%
	100	85	32	64	139.3	-
		95	23.1	46.2	121.6	12.7%
		105	16.94	33.88	109.4	21.5%
		115	12.61	25.22	100.7	27.7%
	200	85	32	64	101.7	-
		95	23.1	46.2	83.9	17.5%
		105	16.94	33.88	71.6	29.6%
		115	12.61	25.22	62.9	38.2%

Thus, the overhead of increasing the oven's temperature is a one-time overhead, whose impact can be further reduced if the volume of the order is large.

Simulation Output for Faults Identified during Testing eDRAM Memory



V. Conclusion

The eDRAM testing mixes up the techniques of SRAM testing and commodity-DRAM testing since eDRAMs use the SRAM interface and DRAM cells. In this paper, we first introduced an exemplary eDRAM design and discussed the key issues which should be emphasized in eDRAM testing by comparing to commodity-DRAM testing and SRAM testing. Then we started from a short SRAM algorithm and discussed the fault models that are not covered by the SRAM testing but should be considered

in eDRAM testing. We also discussed the impact of those faults and how to design a test algorithm to detect them. Furthermore, we analyze the relation between switch transistor's leakage and temperature. Based on that, we can theoretically calculate the equivalent retention time for different temperatures which can be adopted to reduce the retention-test time.

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