Comparative Study of 8T SRAM Cell using CMOS, FinFET and CNTFET in Nanoscale Technologies

Parimala Devi.M, Dr. Sharmila.D, Meenakshi.K
Dept. of ECE, Velalar College of Engineering & Technology, Erode, TN, India
Dept. of EIE, Bannari Amman Institute of Technology, Erode, TN, India
Velalar College of Engineering & Technology, Erode, TN, India

Abstract
In the world of Integrated Circuits, Complementary Metal–Oxide–Semiconductor (CMOS) has lost its credentiality during scaling beyond 32nm. Scaling causes severe Short Channel Effects (SCE) which are difficult to suppress. As a result of such SCE many alternate devices have been studied. Some of the major contestants include Multi Gate Field Effect Transistor (MuGFET) like FinFET and Carbon Nano Tube Field Effect Transistor (CNTFET). In this paper, 8T SRAM cell is analyzed in CMOS, FinFET and CNTFET structures and their performances like standby power Consumption and static noise margin are compared.

Keywords
CMOS, FinFET, CNTFET, Short Channel Effects, Standby Power Consumption, Static Noise Margin

I. Introduction
As MOSFETs are scaled down to nanoscale regime, statistical dopant fluctuations, oxide thickness variations and line edge roughness increase the spread in transistor threshold voltage (Vt) and correspondingly affect the “on” and “off” currents[8]. At sub-45nm channel lengths, achieving a large current drive while maintaining a low off-state leakage becomes challenging [9]. To solve this problem new MOSFET architectures involving the use of multiple gates controlling the transistor have been proposed. FinFET (a self-aligned double-gate MOSFET), CNTFET devices have a straightforward process flow when starting from a conventional bulk transistor. They are the most attractive devices for implementing nanoscale planar MOSFET because of its excellent characteristics such as ideal sub threshold swing, high transconductance (Gm), and reasonable short-channel effect. According to International Technology Roadmap for Semiconductors (ITRS) by the year 2014, 94% of chip area will to be occupied by memory. As memory begins to dominate the circuit delay. Moreover, body in DGFET devices is lightly doped and threshold voltage (Vth) is principally controlled using metal gate work function. The lightly doped body eliminates the Vth variations due to Random Dopant Fluctuation (RDF).

III. SRAM Design Tradeoffs
A. Area vs. Yield
The functionality and density of a memory array are its most important properties. Functionality is guaranteed for large memory arrays by providing sufficiently large design margins, which are determined by device sizing (channel widths and lengths), the supply voltage and, marginally, by the selection of transistor threshold voltages. Although upsizing the transistors increases the noise margins, it increases the cell area and thus lowers the density [15].

B. Read vs. Write Stability
The Read Voltage (Vread) is defined as the minimum voltage the storage nodes can reach during read operation, is determined by the voltage division between a Pull down (PD) transistor and an Access (AC) transistor. The weaker the AC transistor’s driving strength, the smaller Vread is, leading to a larger Read stability. The Write Voltage (Vwrite) is defined as the maximum voltage the storage nodes can reach during write operation, is determined by the voltage division between the AC transistor and the Pull up (PU) transistor. The weaker the AC transistor’s driving strength, the smaller Vwrite is, leading to larger write stability. Thus, a trade-off relationship exists between read stability and write stability.

C. Speed vs. Leakage Current
A fast SRAM cell dissipates low leakage power as required. This is increasingly at odds with a fundamental technology trade-off between transistor speed and leakage: the lower the threshold voltage (Vth) of a transistor, the faster it becomes and the more leakage power it dissipates. As the supply voltage is scaled down, the transistor threshold voltage is also scaled to maintain performance. As a result of the low threshold voltage, leakage power increases rapidly due to the exponential relationship between leakage and Vth. Leakage can be reduced by using higher-Vth transistors, but
by using an all-high-Vth, transistor cell performance degrades by an unacceptable margin.

IV. Novel Devices Based SRAM Design

A. FinFET Technology

The FinFET transistor is a vertical double-gate device and is regarded as a promising alternative for sub-45 nm bulk devices [1]. A unique property of the FinFET is the electrical coupling between the front and back gates. The implication of this coupling is that the threshold voltage of the front gate ($V_{thf}$) is not only established by the process, but also it can be controlled by the Back Gate Voltage ($V_{Gb}$). This is similar to the body effect in a bulk transistor [1].

The distinguishing characteristic of the FinFET is that the conducting channel is wrapped by a thin silicon “fin”, which forms the body of the device. The thickness of the fin (measured in the direction from source to drain) determines the effective channel length of the device.

B. CNTFET Technology

CNTs are sheets of graphene rolled into tubes. Depending on their chirality (i.e., the direction in which the graphene sheet is rolled), the single-walled CNTs can either be metallic or semiconducting. Semiconducting nanotubes have attracted widespread attention of the electron device and circuit designers as a promising channel material for high performance transistors [16].

C. FinFET Based SRAM Design

FinFETs have emerged as the most suitable candidate for DGFET structure. Proper optimization of the FinFET devices is necessary for reducing leakage and improving stability in SRAM. The supply voltage ($VDD$), Fin height ($H_{fin}$) and $V_{th}$ optimization can be used for reducing leakage in FinFET SRAMs by increasing Fin-height which allows reduction in $VDD$. However, reduction in $VDD$ has a strong negative impact on the cell stability under parametric variations. We require a device optimization technique for FinFETs to reduce standby leakage and improve stability in an SRAM cell.
speeds as well. SRAM design at sub-45nm node is challenged by increased short channel effects and sensitivity to process variations. Earlier works [13-14] have shown that FinFET based SRAM design shown improved performance compared to CMOS based design. Functionality and tolerance to process variation are the two important considerations for design of FinFET based SRAM at 32nm technology. Proper functionality is guaranteed by designing the SRAM cell with adequate read, write and static noise margins and lower power consumption.

D. CNTFET Based SRAM Design
The operation of CNFETs based memories is very similar to that of CMOS except for minor differences in device orientation. One such difference being that the source and drain terminals of a CNFET are not interchangeable as is the case with CMOS devices. Care must therefore be taken to orient the transistors in a memory cell in a manner that will ensure correct transmission of logic levels [3].

![Fig. 4: CNTFET Based 8T SRAM Cell](image)

The 8T SRAM cell shown in Figure 7 uses a buffered read to isolate the internal nodes of the cell from the read path. Prior to the read operation the read bit line RBL is precharged to VDD. The read operation is started by asserting the RWL. RBL either remains at VDD (if internal node “q” contains a “0”) or is pulled down to ground (if internal node “q” contains a “1”). In either case, the internal nodes remain undisturbed. Prior to the write operation, the bit lines are precharged to the pre-determined values. The write operation is initiated by asserting the write word line WWL and the nodes attain the corresponding values from the bit lines.

V. Performance Metrics Comparison
The HSPICE using the Predictive Technology Model (PTM) and Stanford University CNTFET model (32nm) is used to simulate the performance of the 8T SRAM cell designed with CMOS, FinFET, and CNTFET based transistors [1]. Table 1 shows the summarized results which compares 8T CNFET SRAM characteristics with FinFET and CMOS SRAM cells.

![Fig. 5: Comparison of Leakage Power of Various 8T SRAM Cells](image)

![Fig. 6: Comparison of Leakage Power of Various 8T SRAM Cells](image)

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>8TCNTFET</th>
<th>8TFinFET</th>
<th>8T CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEAKAGE PWR(nW)</td>
<td>6.34</td>
<td>64.2</td>
<td>114</td>
</tr>
<tr>
<td>WRITE DELAY(ps)</td>
<td>6.6</td>
<td>29.3</td>
<td>36.3</td>
</tr>
<tr>
<td>READ DELAY(ps)</td>
<td>7.16</td>
<td>25.7</td>
<td>23.16</td>
</tr>
<tr>
<td>SNM(mV)</td>
<td>254</td>
<td>202</td>
<td>162</td>
</tr>
</tbody>
</table>

VI. Conclusion
This paper compares CMOS, FinFET and CNTFET 8T SRAM cells using HSPICE simulations. From the comparison table-1, it is inferred that CNTFET 8T SRAM cell shows 11~17 times less leakage power consumption, 5~6 times faster read and write operations, and 1.6 wider SNM than the CMOS, FinFET 8T SRAM cell designs.

VII. Acknowledgement
The authors are very grateful for their respective organizations for their support and encouragement.

References


M. Parimala Devi, a Ph.D. Scholar at the Anna University of Technology Coimbatore, Tamilnadu, India. She has received her M.E. (VLSI Design) from Anna University, Coimbatore India and B.E. (Electronics & Communication Engineering) Degree from the Bharathiyar University Coimbatore, Tamilnadu, and India. She has published many papers in international journals and conferences. Her main research interests are in Low-Power Memory design and Low-Power CMOS Circuit Design, Low-Power High performance analog & digital Circuits.

Dr. D. Sharmila (MISTE, AMIE), Professor & Head in the Department of Electronics & Instrumentation Engineering, Bannari Amman Institute of Technology, Erode, Tamilnadu, India. She is being honored with the Ph.D. in Electronics & Communication Engineering in the Year 2010 from the Anna University, India. She has received his M.E. (Applied Electronics) from Anna University, Chennai, India. and B.E. (Electronics & Communication Engineering) in 1996 from Bharathiyar University, Tamilnadu, India. She has published many papers in international journals and conferences and received 5 best paper awards for her Publications. Her current areas of interest are VLSI and Network Security.

Meenakshi K has received B.E. (Electronics & Communication Engg.) Degree from Anna University, Chennai, India in the year 2006. She joined ISRO as Graduate Trainee in the year 2007. She is pursuing M.E (VLSI Design) in Anna University, Chennai. Her main research interests are Low Power SRAM Design for nanoscale technologies, VLSI Signal Processing and VLSI Design.