Comparison study of Drain Current, Subthreshold Swing and DIBL of III-V Heterostructure and Silicon Double Gate MOSFET

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Abstract

We investigate the performances of 18 nm gate length AlInN/GaN, InP/InGaAs heterostructure and a Silicon double gate MOSFET, using 2D Sentaurus TCAD simulation. The heterostructure device uses lattice-matched wideband $Al_{0.83}In_{0.17}N$ /InP and narrowband GaN / $In_{0.53}Ga_{0.47}As$ layers, along with high-k Al_2O_3 as the gate dielectric, while silicon based device uses SiO_2 gate dielectric. The device has an ultrathin body and is designed according to the ITRS specifications. The simulation is done using the density gradient model and interface traps are also considered. Due to the large two-dimensional electron gas (2DEG) density and high velocity in heterostructure devices, the maximal drain current density achieved is very high. Extensive performance evaluation of the major device has been carried outusing the metrics such as Drain Induced Barrier Lowering (DIBL) and subthreshold slope (SS) for a wide range of gate lengths. The proposed AlInN/GaN and InP/InGaAs heterostructure DG MOSFET shows anexcellent promise as one of the candidates to substitute currently used MOSFETs for future high speed applications.

Keywords

III-V Heterostructure, DIBL, SS, Ultra thinbody(UTB), Narrow Bandgap and wideband gap, Quantum-Well Field Effect Transistors (QWFETs).

I. Introduction

Scaling of the MOSFET to sub 20nm dimensions makes it more complex to maintain the necessary device performance due to significantly increased short channel effects (SCE).To overcome the SCE, device such as thedouble-gate (DG) MOSFET, FinFET and underlap structures are anticipated. The DGMOSFET is gaining popularity as one of the potential candidates of in VLSI research, due to its excellent capacity of being scaled to the shortest channel length by producing an ultrathin body. Also DGMOSFETs have been inthe prime focus for their ultra-low power circuit design due to the improved subthreshold slope and the reduced leakage current compared to bulk CMOS.

Currently, for fast switchingthe device drive current is increasedat lower supply voltage. This leads to an exponentially increasing leakage current, causing unnecessary standby power dissipation [1]. There is a need to explore new channel materials and superior device structures that would present us with energy efficient solutions at high switching speeds. High mobility III-V semiconductors have a significant transport advantage, and are thus are being extensively red as channel materials for upcoming highly scaled CMOS applications. In our previous works we have analysed the performance by varyingthe barrier thickness and the underlap length for heterostructure devices [2-4].

The major motivation of this work is to arrive at a new solution that takes into account both high performance and low leakage, but remains in the quasi-MOS regime which makes it possible to fabricate the device without wide deviation from the existing technology. The new III-V heterostructure underlap device is aimed to achieve high ON state current requirement using bulk conduction arising from high electron mobility transistor (HEMT) like mechanism, and good off-state control by DGMOSFET-like mechanism [5].

The rest of the paper is organized as follows. The description of the device structure is given in Section II. We discuss the device simulation and result discussion in Section III, using standard benchmarking techniques for the evaluation of the device performance. The conclusion is presented in Section IV.

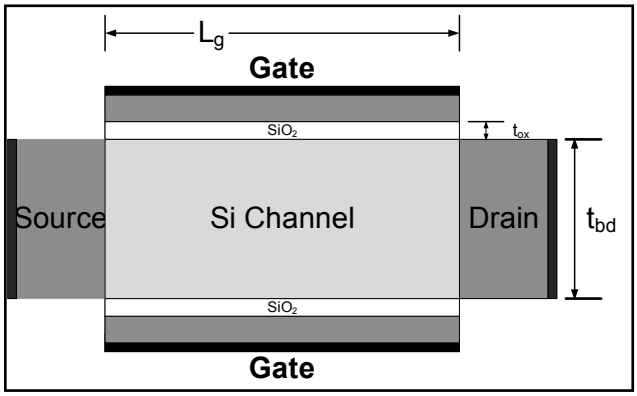

Fig. 1(a): DGMOSFET Consists of Silicon Undoped Channel of Thickness t_{bd} = 6nm, gate length L_g=18nm, and SiO_2oxide thickness t_{ox}=1.2nm. Source/drain region doping is $10^{20}/cm^3$, with 5nm Length

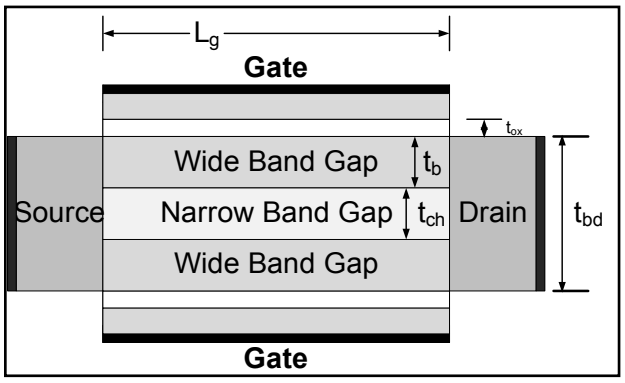

Fig. 1(b): Heterostructure DG MOSFET Consists of Undoped Narrow Bandgap $In_{0.53}Ga_{0.47}As$/GaN(t_{ch} = 4nm) Channel Region and Two Wide Bandgap Barrier InP/ $A_{l0.83}In_{40.17}N$(t_b = 1nm) Regions. Source/Drain Region Doping is $10^{20}cm^3$ with 5nm length. The gate length L_g=18nm and Al_2O_3 gate dielectric with equivalent oxide thickness EOT of 1.2nm

II. Device Structure

We simulate two DG MOSFET devices with gate length L_g=18nm, with an undoped channel Ultra Thin Body (UTB). The device 1(Fig 1.a) channel consists of silicon with body thickness (tbd) of 6nm. The device2 (Fig 1(b)) channel uses III-V Hetero-structure consisting of narrowband $In_{0.53}Ga_{0.47}As$ / GaN layer of 4nm region and two wideband InP/ $A_{l0.83}In_{40.17}N$ (tb) layers of 1nm each. The simulated device structure has source/drain regions doped at 10^{20} cm^3 and uses theabrupt doping at source/drain ends. The source/ drain lengths are 5 nm, the top and bottom gate oxide thickness are t_{ox}= 1.2 nm. Device 1 uses SiO_2 and device 2 uses high-k HfO_2 dielectric to minimize leakages.

Table 1: Characteristics of Materials

Material	GaN (N.B)	$Al_{0.83}In_{40.17}N$ (W.B)	$In_{0.53}Ga_{0.47}As$ (N.B)	InP(W.B)	Si
E_g(eV)	3.4	4.7	0.74	1.344	1.11
Relative Permittivity (ε_r)	9.5	11.7	13.9	12.5	11.68
Lattice Constant (A°)	3.186	3.190	5.868	5.867	5.4307
μ_e (cm^2/Vs)	940	1540	12000	5400	1400
μ_h (cm^2/Vs)	22	82	300	200	450

Physical properties of narrow bandgap and wide bandgap materials and Si are listed in Table 1. Narrow bandgap material is sandwiched between the two wide bandgap barrier layers and the channel is confined at the heterostructure interface. The barrier layer used has the conduction band edge offset with the channel and is nearly lattice matched with the narrowband layer to minimize the traps at its interface with the channel.

An III-V semiconductor has high mobility and thus there is high injection velocity which can increase the ON current with reduction in device delay. However, due to this high mobility the leakage current will also be high. To minimize this leakage high K dielectric such as HfO2 is used in device 2.

The smaller transport mass of III-V material gives higher injection velocity, but the low density of states (DOS) reduces the inversion charge and consequently current [1]. However, due to low effective mass of III-V materials they have high injection velocities, which eventually provides higher drive current. Also, Si implants can be done before the metallization process to minimize the OFF current of III-V based devices.

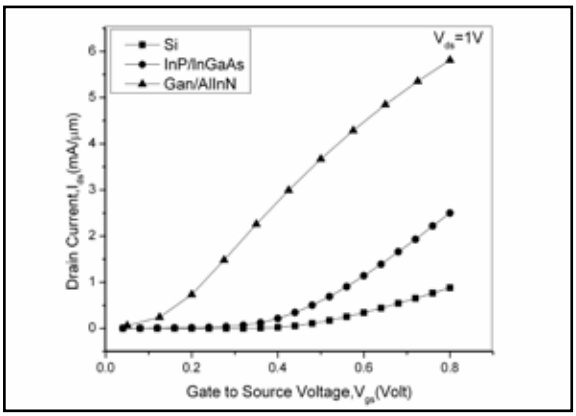

Fig. 2: Transfer Characteristics at V_{ds}=1V for 6nm body thickness, L_g=18nm, t_{ox}=1.2nm, Thickness of $In_{0.53}Ga_{0.47}As$/GaN layer is kept constant at 4nm. Device with t_B= 1nm, provides higher Ids due to larger distance between the oxide and InP/ $Al_{0.83}In_{40.17}N$ Interfacce and the Channel

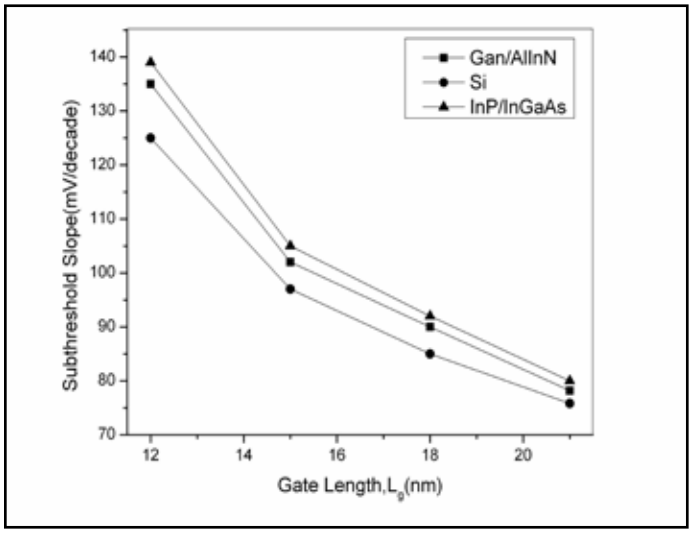

Fig. 3: Subthreshold Slope (SS) Versus Gate Length L_g for Device 1 and Device 2. The Gate Length L_g is Varied from 12nm to 21nm in Steps of 3nm. SS = $\Delta Vg/\Delta (\log_{10} I_D)$

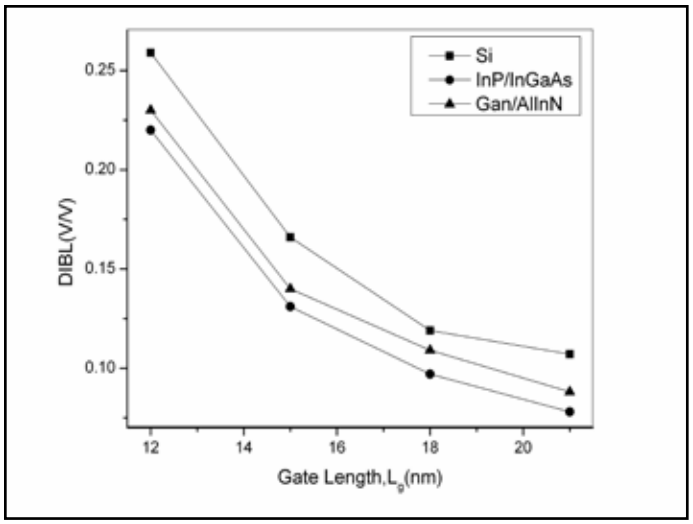

Fig. 4: Dependence of DIBL on Gate Length L_g, for Device 1 and Device 2. The Gate Length L_g is Varied from 12nm to 21nm in Steps of 3nm DIBL=$[(V_{th1}-V_{th2})/(V_{ds1}-V_{ds2})]$ where V_{th1} and V_{th2} are threshold voltages extracted at drain bias of V_{ds1}= 50 mV and V_{ds2}= 1.0 V

III. Device Simulation Results ans Discussion

The device simulation is done using Sentaurus TCAD. The density gradient model used in the simulation, solves the quantum potential equations self consistently with the Poisson equation and carrier continuity equations. The quantum potential is introduced to include quantization effects in a classical device simulation. The density-gradient transport model is used mainly in simulating nanoscale devices, such as single gate MOSFET's, double gate MOSFET, and FinFET structures, the quantization effects is used to analyze the carrier transport in the interface between the two dissimilarBandgap semiconductor material.

III-V compound semiconductor devices are often benchmarked against the presently prevailing silicon devices for determining performance enhancements. We are analyzing the drain current for transportation of charge, subthreshold slope for determining I_{off} of the device and DIBL for performance of electrostatic control over the gate.

Fig. 2 shows thetypical output and transfer characteristics of both the devices with L_g=18nm. We can find excellent characteristics

clearly depicting higher drain level for III-V Heterostructure device, arising from high mobility of carriers. The drain current is approximately three times containing InP/InGaAs and seven times containing AlInN/GaN higher for device2 as compared with device 1. The barrier layer effectively confines the charge in the narrow bandgap high mobility region and also overcomes the interface state effect D_{it}. Since the nitride based device has higher spontaneous polarization that indicate the formation of maximum 2DEG charge generated without applied of external electric field. Thus the maximum drain current is obtained for the nitride based devices.

Fig. 3 and 4 show Subthreshold Slope (SS) and Drain induced Barrier Lowering (DIBL) with variation of gate length (L_g) respectively. A decrease in SS and DIBL is observed by increasing channel length due to decrease in current. The subthreshold slope reduced for device 1 as compared with device 2 because of decrease in effective oxide thickness. However, the DIBL for device 2 is less as compared to device 1, that identifies the electrostatic control of gate is more in the case of device2.

IV. Conclusion

A performance investigation of AlInN/GaN, InP/InGaAs heterostructures and Silicon DG MOSFETs is done for major device metrics like DIBL and SS, for a wide range of gate lengths. Lattice matched $Al_{0.83}In_{0.17}N$ /GaN and InP/$In_{0.53}Ga_{0.47}As$ have much larger conductionband discontinuity and also stronger spontaneous polarizationeffects, giving higher 2DEG charge density. The heterostructure interface provides high carrier velocity and mobility. An impressive drain current density is obtained in case of nitide based devices with a gate length of 18 nm due to more spontaneous polarization effect. DIBL dependence onLgis more for lower gate length and becomes less for a longer gate length. The SS performance is degraded because the buried channel is away fromthe gate dielectric interface. The results show that there is a need to optimize the DIBLand SS values for the specific logic design. TheAlInN/GaN heterostructure underlap DG MOSFET shows excellent promise as one of the candidates to substitute present MOSFETs for future high-speed applications.

V. Acknowledgment

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