Design and Analysis of 2:1 Multiplexer for High Performance Digital Systems

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Abstract
This paper is based on pre layout simulations of a proposed design of 2:1 multiplexer circuit that shows improved performance than the existing 2:1 multiplexer circuit. The proposed design demonstrates the superiority in terms of power–delay product, temperature sustainability and frequency when compared with existing 2:1 multiplexer and comparative analysis on 90nm and 45nm standard model on Tanner EDA tool version 13.0.

Keywords
CMOS Logic, 2:1 Multiplexer, Low Power, DCVSL and VLSI

I. Introduction

Advances in CMOS technology have led to a renewed interest in the design of basic functional units for digital systems. The use of integrated circuits in high performance computing, telecommunications, and consumer electronics has been growing at a very fast pace. This trend is expected to continue, with very important implications for power-efficient VLSI and systems designs. Digital integrated circuits commonly use CMOS circuits as building blocks. The continuing decrease in feature size of CMOS circuits and corresponding increase in chip density and operating frequency have made power consumption a major concern in VLSI design. Excessive power dissipation in integrated circuits not only discourages their use in portable environment but also causes overheating which reduces chip life and degrades performance [1-2]. 2:1 multiplexer is an important element in many variant circuit designs, such as the implementation of an FPGA and memory circuits. This is especially useful in situations when cost is a factor and for modularity. Therefore study on multiplexer is inevitable and any modifications made to the 2:1 multiplexer would affect the system as a whole. The rest of the paper is organized as follows: Section II describes the operation of existing 2:1 multiplexer as reported in the literature. Section III describes the proposed 2:1 multiplexer design in detail. Pre layout simulation results are discussed Section IV, presents the simulation results and conclusions are drawn in Section V.

II. Prior work

In this paper, we explore the Differential Cascode Voltage-Switch Logic (DCVSL) circuit design methodology. The key benefits of DCVSL are consumes no static power (like standard CMOS), uses latch to compute output quickly, requires true/complement inputs, produces true/complement outputs [2-4]. Allows "Complex" gates, never needs inverters in the logic path and low power consumption. A logic function and its inverse are automatically implemented in this logic style [4-5].

Table 1: Truth Table of 2:1 Multiplexer

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

The schematic diagram of existing DCVSL 2:1multiplexer is shown in fig. 1. The pull-down network implemented by the NMOS logic tree generates complementary output. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. It can be divided it to two basic parts: a differential latching circuit and a cascoded complementary logic array [6-9].

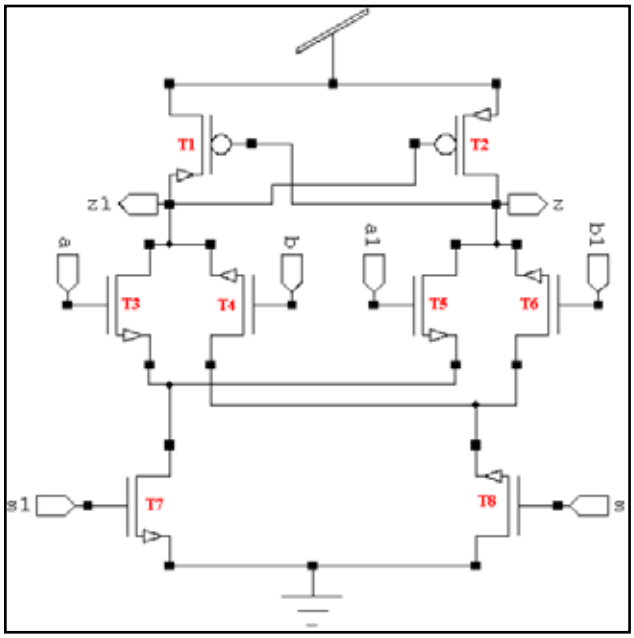

Fig. 1: Schematic of Existing 2:1 Multiplexer

III. Proposed 2:1 Multiplexer Design

By adding two NMOS transistors T1 and T4 in the pull up part of existing 2:1 multiplexer the circuit shows a remarkable improvement over the existing design. In the proposed circuit due to the excess added transistors there is a reduction in threshold loss for the circuit, which further causes the reduction in overall power consumption of the circuit. Due to the transmission gate topology in the proposed design the circuit shows better output waveforms in terms of threshold loss as shown in fig. 11. The two logic trees are capable of processing complex functions within a single circuit delay. The schematic of proposed 2:1multiplexer is shown in fig. 2.

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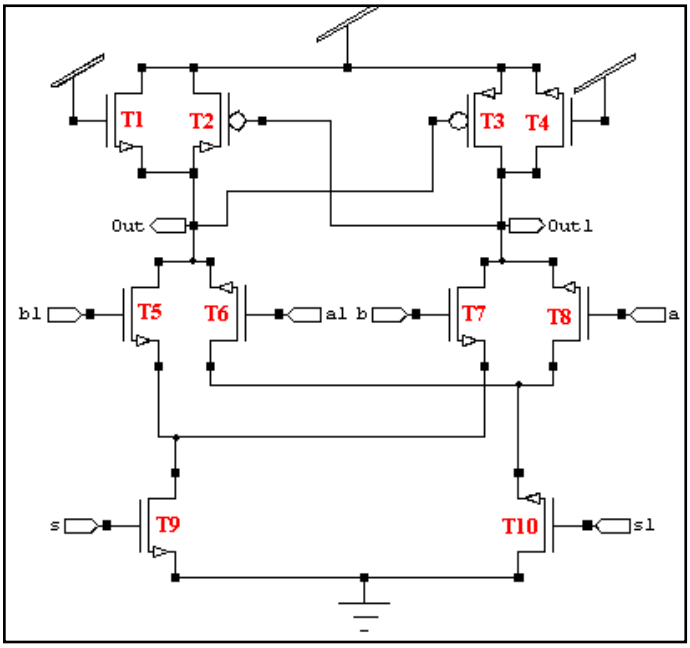

Fig. 2: Schematic of Proposed 2:1 Multiplexer

IV. Simulations and Comparison

All schematic simulations are performed on Tanner EDA tool version 13.0 using 90nm and 45nm technology with input voltage ranges from 0.6V to 1.4 V. In order to prove that proposed design is consuming low power and have high performance, simulations are carried out for power-delay product at increasing input voltage, operating frequency and temperature. To establish an impartial testing environment all circuits have been tested on the same input patterns which covers all combinations of the input stream. From the fig. 3 and fig. 7, reveals that the power consumption performance of the proposed 2:1 multiplexer is remarkably reduced than the existing 2:1 multiplexer. Proposed 2:1 multiplexer shows slightly less delay than the delay of existing 2:1 multiplexer for input voltage ranging from 0.6V to 1.4V which shown in figure4 and figure8. Similar results for power consumption vs. frequency and power consumption vs. temperature are shown in fig. 5, fig. 6 and fig. 9, fig. 10, respectively. Table 2, & Table 3, show the power delay product over a range of power supply voltages and as it is shown in the table that proposed 2:1 multiplexer circuit show minimum power delay product.

A. At 90 nm Technology

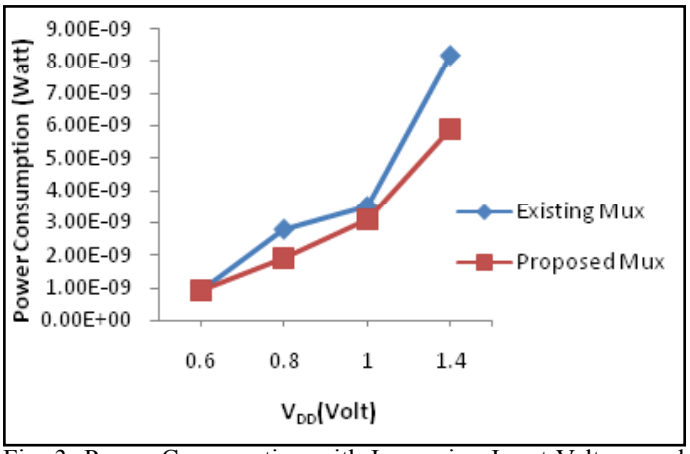

Fig. 3: Power Consumption with Increasing Input Voltage and Supply Voltage

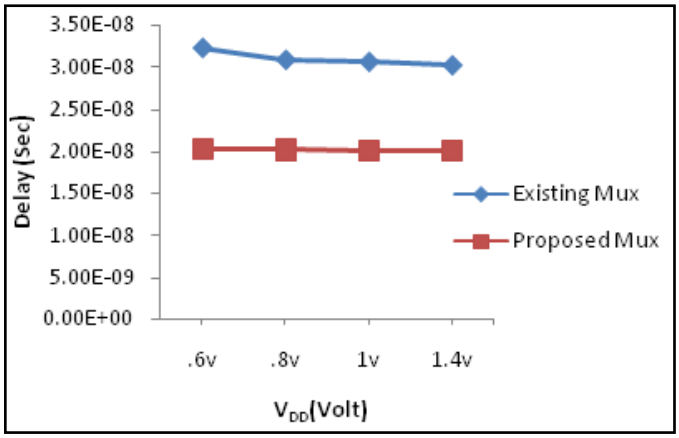

Fig. 4: Delay Comparison with Increasing Input Voltage

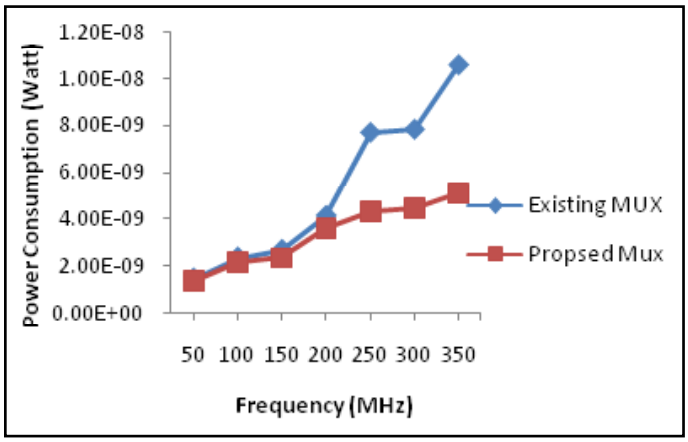

Fig. 5: Power Consumption Comparison with Increasing Operating Frequency at 1V Input Voltage and Supply Voltage

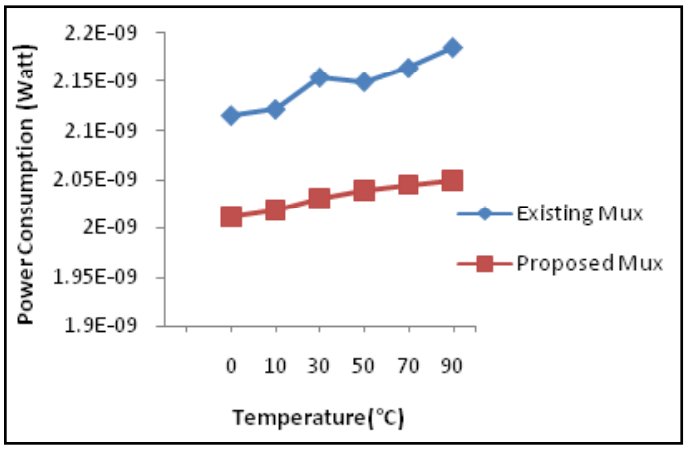

Fig. 6: Power Consumption with Varying Temperature at 1V Input Voltage and Supply Voltage

Table 2: Power Delay Product Comparison of Existing and Proposed 2:1 Multiplexer Structure

V_{DD} (volts)	Power Delay Product(Watt-sec) (90nm)	
	Existing Mux	Proposed Mux
.6	2.96492E-17	1.82617E-17
.8	8.62683E-17	3.82869E-17
1	1.07446E-16	6.25955E-17
1.4	2.46808E-16	1.1905E-16

B. At 45 nm Technology

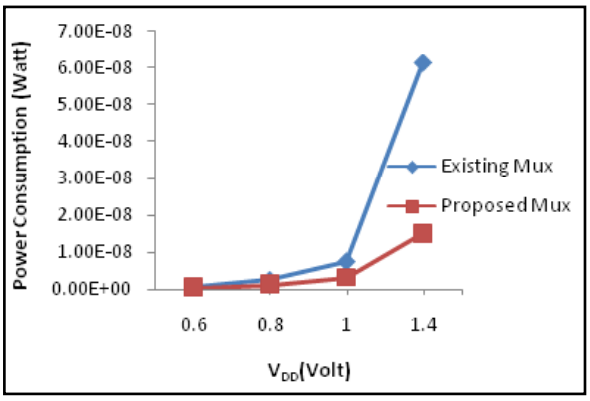

Fig. 7: Power Consumption with Increasing Input Voltage and Supply Voltage

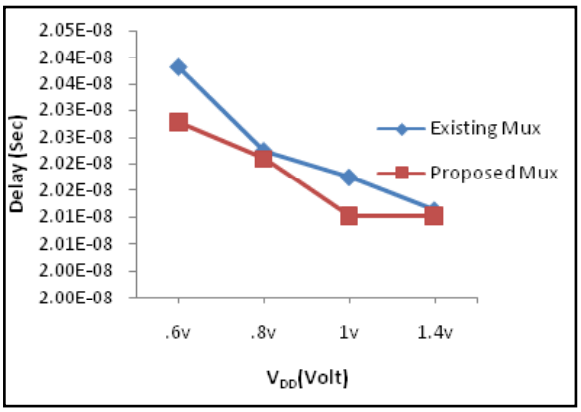

Fig. 8: Delay Comparison with Increasing Input Voltage

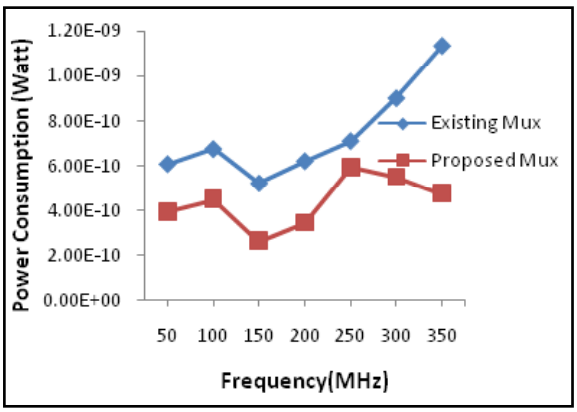

Fig. 9: Power Consumption Comparison with Increasing Operating Frequency at 1V Input Voltage and Supply Voltage

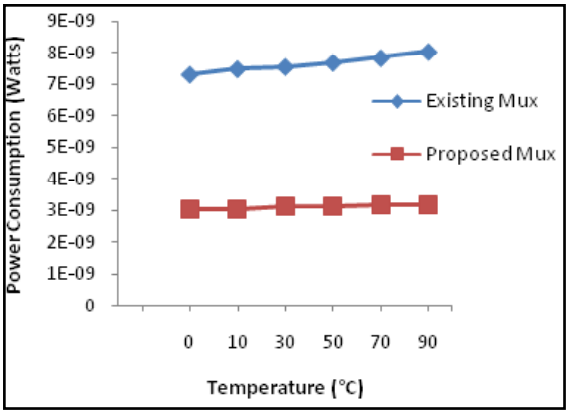

Fig. 10: Power Consumption with Varying Temperature at 1V Input Voltage and Supply Voltage

Table 3: Power Delay Product Comparison of Existing and Proposed 2:1 Multiplexer Structure

V_{DD} (volts)	Power Delay Product(Watt-sec) (45nm)	
	Existing Mux	Proposed Mux
.6	1.24106E-17	7.99194E-18
.8	5.09886E-17	2.59553E-17
1	1.51653E-16	6.34903E-17
1.4	1.23817E-15	3.01982E-16

V. Conclusion

The proposed 2:1 multiplexer is found to give better performance than the existing 2:1 multiplexer. The proposed circuit has been tested to have better temperature sustainability, frequency and significantly less power-delay product to achieve high performance. The proposed 2:1 multiplexer has been designed and studied using 90nm technology and proved it to be a better option for low power complex system design. It shows remarkable improvement in power delay product. The net effect is that proposed 2:1 multiplexer shows a much better performance compared to existing 2:1 multiplexer.

References

[1] A. Bellaouar, Mohamed I. Elmasry,"Low-power digital VLSI design: circuits and systems", 2nd Edition.

[2] Kang, Sung-Mo, Leblebici, Yusuf,"CMOS Digital Integrated Circuits Analysis and Design", McGraw-Hill International Editions, Boston, 2nd Edition, 1999.

[3] D. Z. Turker, S. P.Khatri,"A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Applications", IEEE transactions on circuits and systems june 2011, Vol. 58, No. 6, pp. 1125-1138.

[4] F-s Lai, W Hwang,"Design and Implementation of Differential Cascode Voltage Switch with Pass-Gate (DCVSPG) Logic for High-Performance Digital Systems", IEEE journal of solid-state circuits, Vol. 32, No. 4, April 1997, pp. 563-573.

[5] P. K. Lala, A. Walker,"A Fine Grain Configurable Logic Block for Self-checking FPGAs",VLSI Design 2001, Vol. 12, No. 4, pp. 527-536.

[6] Jan M. Rabaey,"Digital Integrated Circuits", a design prospective, Upper Saddle River: Prentice-Hall, 1996.

[7] Heller, L. G. et al.,"Cascode Voltage Switch Logic: A differential CMOS Logic Family", proceedings of 1984 IEEE International Solid-state Circuits Conference, pp. 16-17.

[8] Ila Gupta, Neha Arora, Prof.B.P.Singh,"Simulation and Analysis of 2:1 Multiplexer Circuits at 90nm Technology", in International Journal of Modern Engineering Research, Vol. 1, Issue. 2, pp. 642-647, 2011.

[9] Ila Gupta, Neha Arora, Prof.B.P.Singh,"Analysis of Several 2:1 Multiplexer Circuits at 90nm and 45nm Technologies" International Journal of Scientific and Research Publications, Vol. 2, Issue 2, 2012.

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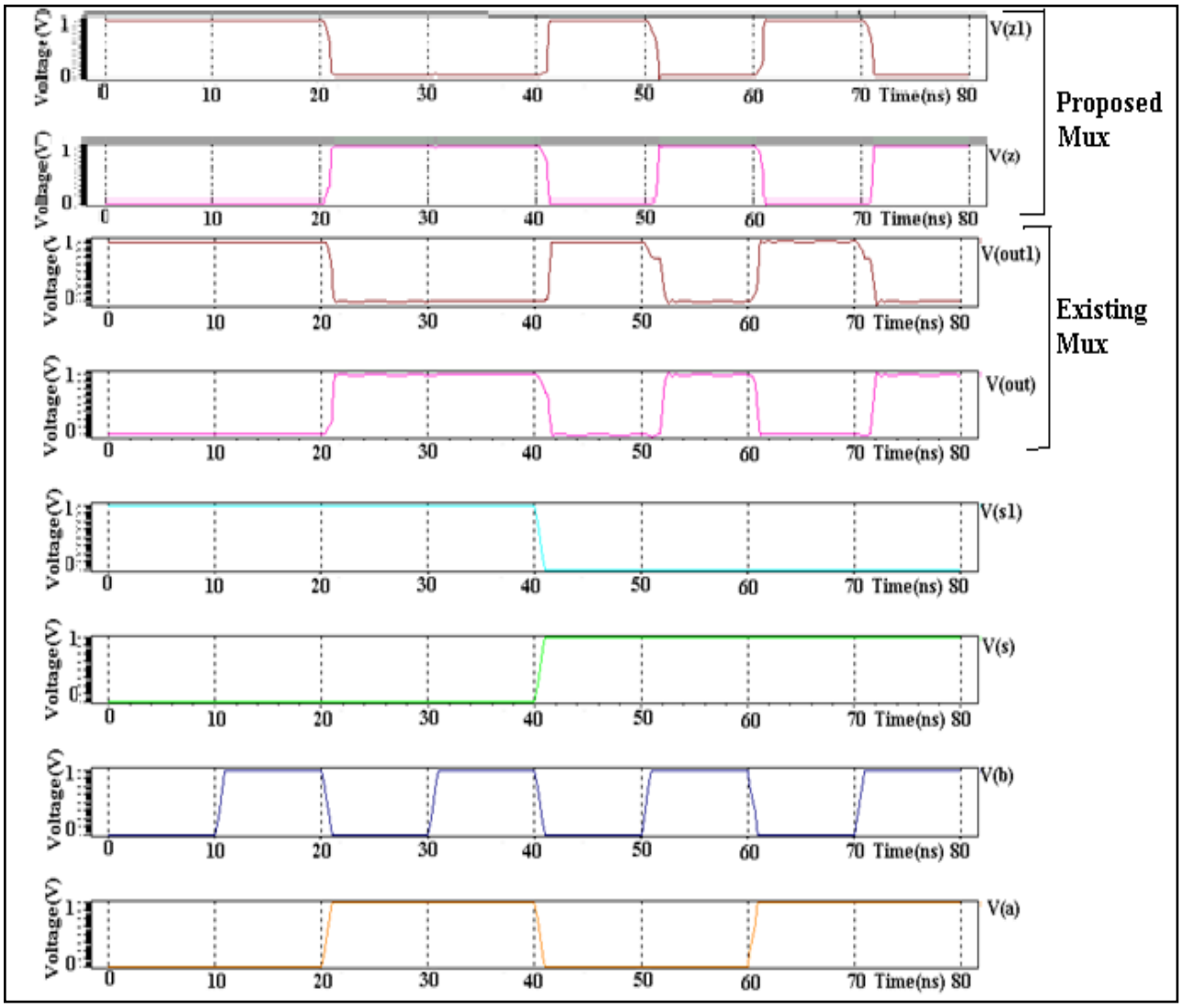

Fig. 11: In-Out Waveforms of Existing 2:1 Multiplexer and Proposed 2:1 Multiplexer

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