Comparative Study of Single Phase PLL Algorithms for Grid Synchronization Applications

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Abstract

Phase Locked Loop is a control system technique that is used extensively for synchronization purposes in diverse fields, most importantly in communication systems and in power electronics. Owing to its significance, the PLL has been a subject of great interest and various schemes and their improvements have been proposed for its implementation. This paper serves to elaborate on and compare the performance of four prevalent PLL schemes, the Zero Crossing Detector based PLL, Inverse Park based PLL, Second Order Generalized Integrator based PLL and the Enhanced Phase Locked Loop. The Zero Crossing Detector based PLL detects the phase error between its output and the reference at every zero crossing and corrects for it. The Inverse Park PLL and the SOGI PLL differ only in the way they generate the orthogonal signals that are fed to the phase detector. The Enhanced PLL is based on the Adaptive Filter theory.

Keywords

Single Phase PLL, Inverse Park PLL, SOGI PLL, Enhanced PLL

I. Introduction

Automatic synchronization of electronic oscillators was first described by Appleton in 1923. The concept of the Phase Locked Loop was proposed by H. de Bellescise in 1932 based on which British researchers developed a simpler alternative to the Superheterodyne Receiver. It was immediately put to use in radio communication systems and analog television receivers. The Phase Locked Loop however, was put to widespread use after the advent of Signetics monolithic IC based Phase Locked Loop systems. Today PLLs are extensively used in various industrial fields such as communication systems, motor control systems, induction heating power supplies and contactless power supplies. Recently, PLL techniques are being used in grid-interfaced converters. For efficient power transmission to the grid, it is essential that the inverter is synchronized with the utility grid for a power factor that is close to unity. The Phase Locked Loop is being extensively used as the synchronization algorithm in these inverters.

II. PLL Basics

The phase locked loop structure [1-2] is a feedback control system that automatically adjusts the phase of a locally generated signal to match the phase of an input signal. In grid connected systems, the purpose of a PLL is to synchronize the instantaneous phase angle of the inverter voltage \(v_{inv}\) with the phase angle of the grid voltage \(v_{grid}\) in order to obtain a power factor as close to unity as possible. A PLL alters the inverter voltage frequency \(\omega_{inv}\) if the inverter output and the grid voltage are out of phase due to a sudden change in the loading condition at the utility grid so that they are in phase. Figure 1 shows the block diagram of a typical grid connected inverter that employs a PLL as a synchronization method.
B. Single Phase Inverse Park PLL

The Inverse Park PLL resembles the Synchronized frame PLL design [3] which is used for three phase systems. In a Synchronized Frame PLL, the three phase signal is converted to the (α-β) stationary reference frame by using the Clarke transformation. The Park transformation is then used to convert the stationary reference frame to a rotating reference frame. The Direct (d) or the Quadrature (q) axis component is then fed to a PI controller having a reference of zero. The PI controller output is integrated to get the estimated instantaneous phase angle for the PLL output signal. The estimated instantaneous phase angle is fed back to the Clarke and Park transforms. The estimated phase angle gets synchronized with the instantaneous phase angle of the utility grid once the d or q axis output is driven to zero. It is explained in the following derivation.

Denoting the Clarke transformation outputs as,

\[ V_\alpha = V_{\text{in}} \cdot \sin(\theta) \]  
\[ V_\beta = -V_{\text{in}} \cdot \sin \left( \theta - \frac{\pi}{2} \right) \]  

The Park transformation outputs can be denoted as,

\[ V_d = V_\alpha \cdot \sin(\theta') + V_\beta \cdot \cos(\theta') \]  
\[ V_q = -V_\alpha \cdot \cos(\theta') + V_\beta \cdot \sin(\theta') \]  

Substituting equations (1), (2) in (3),(4), we get,

\[ V_d = V_{\text{in}} \cdot \sin(\theta') \sin(\theta) - V_{\text{in}} \cdot \sin \left( \theta - \frac{\pi}{2} \right) \cos(\theta') \]  
\[ V_q = -V_{\text{in}} \cdot \cos(\theta') \sin(\theta) - V_{\text{in}} \cdot \sin \left( \theta - \frac{\pi}{2} \right) \sin(\theta') \]  

Equation (4) can be rewritten as,

\[ V_q = -V_{\text{in}} \cdot \sin(\theta) \cos(\theta') + V_{\text{in}} \cdot \cos(\theta) \sin(\theta') \]  

Therefore, solving for \( V_q = 0 \), we get \( \theta = \theta' + 2n\pi \), which for practical purposes, can be written as \( \theta = \theta' \). Hence, the estimated instantaneous phase angle, \( \theta' \), is equal to the grid phase angle, \( \theta \), when the q-axis output of the Park transform block, which acts as the phase detector, is zero. For a single phase system, the PLL structure is modified as mentioned in [4]. The Clarke transformation block is replaced by an Orthogonal Signal Generator, whose block diagram is shown in fig. 4.

The Grid reference signal is fed as \( V_\alpha \) while \( V_\beta \) is internally generated. The outputs of the Park transform block are passed through single order filters which act as lag blocks, before being fed to the Inverse Park Transform block. The \( \beta \)-axis block is fed back to the Park transform block mentioned earlier. The \( V_\alpha \) and \( V_\beta \) signals are passed to the Park transform block which acts as the Phase Detector(PD) in the PLL. The output of the PD is then passed to the PI controller, whose output is integrated to get the estimated phase angle. The overall structure of the Inverse Park PLL is shown in fig. 5.

C. Second Order Generalized Integrator based PLL

The structure of the SOGI based PLL [5] differs from the Inverse Park based PLL in the way the orthogonal signals are produced. The structure of the SOGI is shown in fig. 6. As output signals, two sine waves \( V' \) and \( qV' \), with a phase shift of \( \pi/2 \) are generated. The component \( V' \) has the same phase and amplitude as the fundamental of the input voltage signal (\( V \)).

The closed loop transfer functions \( H_d(V'/V) \) and \( H_q(qV'/V) \) are defined as follows:

\[ H_d(s) = \frac{V'}{V}(s) = \frac{k_\omega_n s}{s^2 + k_\omega_n s + \omega_n^2} \]  
\[ H_q(s) = \frac{qV'}{V}(s) = \frac{k_\omega_n}{s^2 + k_\omega_n s + \omega_n^2} \]  

where \( \omega_n \) is the angular frequency of the signal and \( k \) is a constant that determines the bandwidth of the filters.
As can be seen, the transfer function for $H_d$ resembles that of a Band Pass Filter, that filters out harmonic and random noise and whose output is in phase with that of the input signal. The transfer function for $H_q$ is the same as that of a second order Low Pass Filter, that not only filters out harmonics and random noise, but also introduces a phase shift of $\pi/2$ radians. Figure 7 shows the block diagram of the overall PLL structure.

**Fig. 7: Structure of SOGI based PLL**

The performance of the SOGI orthogonal signal generator is dependent on the term $\omega_n$ which is the angular frequency of the signal. Thus, it is calculated and adjusted in the SOGI by the PLL in order to make it frequency adaptive. Like the Inverse Park PLL, the SOGI PLL can filter out noise and harmonics but is susceptible to a DC bias in the voltage signal.

### D. Enhanced PLL

The enhanced phase locked loop [6-7] is frequency-adaptive and has a non-linear phase detector. Figure 8 shows the block diagram of the Enhanced PLL.

**Fig. 8: Block Diagram of Enhanced PLL**

The EPLL is based on adaptive filter theory. An adaptive filter is a filter that self-adjusts its transfer function according to an optimization algorithm driven by an error signal. The error signal in this case is the difference between the estimated and the reference signal and the optimization algorithm is the steepest descent method. Figure 9 shows the block diagram of a typical Adaptive Notch Filter.

**Fig. 9: Block Diagram of an Adaptive Notch Filter**

From fig. 10, one can see that assuming $V_{in} = A\sin(\omega t + \theta)$, $V_{out} = 0$ when $\theta' = \omega t + \theta$. Hence, the above ANF can be used as the Phase Detector for a PLL. Fig. 10 shows the block diagram of an EPLL segregated into the parts of a generic PLL.

**Fig. 10: Block Diagram of Enhanced PLL**

Its major improvement over conventional PLLs is the PD mechanism which provides information about the frequency, phase angle and amplitude. The constant $K$ controls the speed of amplitude convergence while $k_p$ and $k_i$ control the rates of frequency and phase convergence. An EPLL can provide higher degree of immunity and insensitivity to noise and harmonics in the input signal. It is an effective method for synchronization of the grid-interfaced converters in polluted and variable-frequency environments.

### IV. System Modeling and Simulation

The aforementioned PLLs were modeled using SIMULINK.

**Fig. 11: Zero Crossing Detector based PLL**
Fig. 11 shows the SIMULINK model of a Zero Crossing Detector based PLL. Fig. 12(a) shows the model of the Inverse Park PLL. Fig. 12(b) shows the Orthogonal System Generator subsystem. Fig. 13(a), (b) show the SOGI based PLL and the SOGI OSG subsystem, respectively. Fig. 14 shows the model of the Enhanced PLL.

V. Experiments and Results

A. Susceptibility to Random Noise
Uniform noise, having a maximum magnitude of 10% and 33% of the input voltage is added to the input signal. Fig. 15 shows the input signal without any noise added.
Fig. 16: (a) Input signal with 10% noise. (b) Zero Crossing Detector. (c) Inverse Park PLL response. (d) SOGI PLL response. (e) Enhanced PLL response.

Fig. 16 shows the response of the PLL models to 10% noise. The distortion in the outputs of each of the PLL models other than the ZCD is negligible and is slightly visible only in the case of the Inverse Park PLL. The noise in the signal leads to multiple unwanted zero crossings, disrupting the functioning of the ZCD.

Fig. 17: (a) Input signal with 33% noise. (b) Zero Crossing Detector. (c) Inverse Park PLL response. (d) SOGI PLL response. (e) Enhanced PLL response.

Fig. 17 shows the response of the PLL models to 30% noise. Other than the ZCD PLL, the Inverse Park PLL is most susceptible to noise distortions among the three, whereas the Enhanced PLL shows little distortions in its output. Distortion in the SOGI PLL output is visible but is relatively less than that of the Inverse Park PLL. The Zero Crossing Detector gives a completely disrupted output as expected.

**B. Response to Change in Frequency**

The PLL models are then subjected to a frequency jump of 6 Hz from 47 Hz to 53 Hz. The $K_p$ and $K_i$ constants of their control loops are given the same values.
C. Response to Voltage Sag

The input signal is subjected to voltage sag of 33% and the response of the PLL models is plotted.
As can be seen in Figure 19 (b) and (c), the change in the amplitude of Inverse Park PLL and the SOGI PLL is almost instantaneous. This can be slowed down by adding a low-pass filter. Figure 19(d), (e) show how the value of K in an EPLL affects the amplitude convergence time. The RMS method of determining amplitude of the ZCD is too slow when the RMS is taken over the whole wave. This can be rectified by taking the RMS of the amplitude over an individual cycle.

D. Harmonic Distortion

Fig. 20 shows the time response of the PLLs to a 40% 2nd harmonic injected in the input signal.

The Inverse Park PLL shows the maximum distortion whereas the Enhanced PLL is practically immune and has the lowest sensitivity. The ZCD’s measured frequency is twice that of the signal owing to the additional zero crossing in a cycle.

E. Distortion Due to DC Voltage Offset in Input

A DC bias of 33% is added to the input. Fig. 21 shows the response of the PLL models.
As can be seen, the Inverse Park PLL and the SOGI PLL show significant distortion in their output, with that of the Inverse Park PLL being the most visible. The output of the Enhanced PLL is practically immune to the DC voltage offset. A DC bias disrupts the fundamental principle of a ZCD because the zero crossings no longer occur at the end of each half cycle.

VI. Conclusion
In this work, four existing algorithms for single phase PLLs have been briefly reviewed. They have been modeled using MATLAB-SIMULINK and their response to aforementioned disturbances have been simulated and presented. It has been observed that despite its complexity relative to the ZCD PLL, SOGI PLL and the Inverse Park PLL, the Enhanced Phase Locked Loop is the least sensitive to distortion due to DC bias and harmonic and random noise in the input and is thus suited for use in practical applications in noisy conditions. Although the implementation of the ZCD is quite simple, one has to devise methods to filter out bias, noise and any harmonic distortions in the input in order to get it to work in real, noisy conditions.

VII. Appendix
Abbreviations and symbols used:
PLL: Phase Locked Loop
PD: Phase Detector
VCO: Voltage Controlled Oscillator
ZCD: Zero Crossing Detector
SOGI: Second Order Generalized Integrator
OSG: Orthogonal System Generator
EPLL: Enhanced Phase Locked Loop
θ: Measured Phase Angle/Phase Angle of the Input Signal
θ*: Phase Angle of the PLL output
ω: Angular Frequency
V: Voltage

References

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