A Novel 7-Level Parallel Current Source Inverter for High Power Application with DC Current Balance Control

M. Vamsi Sree, M. R. P. Reddy, CH. Rambabu
1,2,3Dept. of EEE, Sri Vasavi Engineering College, Tadepalligudem, AP, India

Abstract

Multilevel inverters are increasingly being used in high power medium voltage applications when compared to two level inverter due to their merits, such as lower common mode voltage, lower dv/dt, lower harmonics in output voltage and current. Among various modulation techniques for a multilevel inverter, space vector pulse width modulation is popular due to the merits like, it directly uses the control variable given by the control system and identifies each switching vector as a point in complex space. However, the implementation of the SVPWM for a multilevel inverter is complicated. The complexity is due to the difficulty in determining the location of the reference vector, the calculations of on times and the determination and selection of switching states. The multilevel SVPWM method uses the concepts of two level modulations to calculate the on times of an n-level inverter. Use of multilevel inverters has become popular for motor drive applications. In this paper, a novel Space Vector Modulation is introduced for a 5-level & 7-level parallel current source inverter with DC current balance control is proposed. The method is working by synthesizing the rotating current reference vector in the inverter’s space vector plane with three adjacent switching vectors. One Medium vector is employed as one of adjacent vectors to balance the input DC currents. The switching state for each switching vector is chosen to provide the balanced DC link currents. In addition, lower switching frequency is achievable due to switching design which minimizes the switching loss. Finally, effectiveness of the proposed method is verified by simulation.

Keywords

Multi-level Current Source Inverter, Space Vector Modulation, DC Current Balance Control, High Power

I. Introduction

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. One advantage that Multi level inverters have compared to two level inverters is minimum harmonic distortion. A multilevel inverter can be utilized for multipurpose applications, such as an active power filter, a static VAR compensator and machine drive for sinusoidal and trapezoidal current applications. Some drawbacks to the multilevel inverters are the need for isolated power supplies for each one of the stages, they are more expensive, and they are more difficult to control in software.

One of the significant advantages of multilevel configuration is the harmonics reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [2-3]. These multilevel inverters, in case of m-level, can increase the capacity by (m-1) times than that of two-level inverter through the series connection of power semiconductor devices without additional circuit to have uniform voltage sharing. Comparing with two level inverter system having the same capacity, multilevel inverters have the advantages that the harmonic components of line-to-line voltages fed to load, switching frequency of the devices and EMI problem could be decreased [1].

Power electronic inverters are widely used in various industrial drive applications. To overcome the problems of the limited voltage and current ratings of power semiconductors devices, some kinds of series and/or parallel connections are necessary. Recently, the multilevel inverters have received more attention in literature due to their ability to synthesize waveforms with a better harmonic spectrum and to attain higher voltages. They are applied in many industrial applications such as ac power supplies, static Var compensators, and drive system, etc. The output voltage waveform of a multilevel inverter is composed of a number of levels of voltages starting form three levels and reaching infinity depending upon the number of the DC sources. The main function of a multilevel inverter is to produce a desired ac voltage waveform from several levels of DC voltage sources. These DC voltages may or may not be equal to one another. These DC sources can be obtained from batteries, fuel cells, or solar cells. Conventionally, each phase of a cascaded multilevel converter requires ‘n’ DC sources for 2n + 1 levels in applications that involve real power transfer. These DC sources are assumed to have identical amplitudes.

In comparison to VSI drives, CSI drives have simpler topology with lower switch count, more friendly waveforms and reliable over current and short-circuit protection. CSI drive uses GCT switches and PWM strategies are applied to have an acceptable input and output waveforms. CSI drive has a great harmonics performance using the SHE switching modulation and acceptable dynamic response using SVM strategy [2]. Different switching strategies make distinctive performances in which they may be applied in industry. It is of a great significance to analyze each of these features in order to use them where matched by the industry demand. Generally speaking, SHE switching strategy provides higher harmonics performance whereas SVM switching pattern brings higher dynamic performance to converter.

Industry demand for higher power range and superior performance provide vast field for new converters which are a combination of conventional converters. This way, multi-level and multi-module converters came up. There is no doubt that multi-level converters have become as accepted and thus commercially available alternative. The main feature of multi-level current source converters is providing higher range of power. Employing specific configurations and applying moderated switching modulations brings higher performance and consequently more industry applications.

On the other hand, increased size, mass and higher cost is inevitable. In addition, augmented control methods must be employed to eliminate unwanted and adverse phenomena such as circulating current and unbalance DC currents. In this report, a novel Space Vector Modulation SVM switching scheme is introduced for a 5-level and 7-level inverter with DC current balance control that brings superior harmonic at higher modulation indices and dynamic performance.
II. Proposed Configurations

The employed configuration is a back to back Current Source Converter CSC, which is constituted by a single level Current Source Rectifier CSR and a multi-level Current Source Inverter CSI which is built up by two parallel current source inverters. Fig. 1 illustrates the designed model block diagram.

![Fig. 1: System Block Diagram](image1)

Input is a three phase AC voltage through a three phase line which is modeled with a resistance and an inductance in series. A three phase capacitors is used in the input terminal of CSR which assists commutation process and provides harmonic filter. However, there may be LC resonances problem in addition to the affected input power factor. The value of the capacitor per phase depends on the switching frequency, the input power factor, LC resonant mode, and required line current THD. Normally it would be in the range of 0.3 to 0.6 pu for high power rectifiers operating with a switching frequency of a few hundred Hz. [1] Six switches (GCT), two switches per leg, constitute the CSR. When the rectifier is used as a front end in high power MV drives, two or more GCTs can be connected in series to prove higher range of voltage. A DC choke \( L_d \) per each DC link is required to maintain the dc output current in an acceptable range which has less than 15% ripples. The size of the DC choke is normally in the range of 0.5 to 0.8 pu. [1] According to the application needs and limitation, including harmonics performance and THD, \( \frac{dv}{dt} \), dynamic response and etc, one may appreciate appropriate switching modulation. Selected harmonics elimination SHE modulation is employed to produce the DC current and to eliminate 5th, 7th and 11th harmonics on the AC side. In addition, the closed loop PI controller is employed to maintain the dc current at the desired value (i.e. 220A) through delay angle \( \alpha \) control.

Two parallel single bridge inverters constitute the 5 level current source inverter. Fig. 3 illustrates a single bridge current source inverter CSI. Fig. 4 illustrates a 5-level current source inverter CSI. Input is a DC current which comes from a rectifier through four dc inductances \( L_{d1} - L_{d4} \).

![Fig. 2: Single Bridge Current Source Rectifier](image2)

![Fig. 3: Single Bridge Current Source Inverter](image3)

![Fig. 4: Five-Level Current Source Inverter](image4)
half, excluding commutation intervals. Space Vector Modulation (SVM) is employed to produce ac current at the load side. The switching pattern is designed to bring low harmonic content and high dynamic performance simultaneously. In addition, the closed loop PI controller is employed to maintain the output voltage at a desired value.

### III. Space Vector Modulation

There are so many modulation techniques are available, one of the new breed of PWM method is the Space Vector Modulation (SVPWM). This modulation method presents important advantages compared with PWM modulation. As it was seen before, PWM modulation calculates the multilevel converter switching configurations automatically. In fact, it is an automatic method that completely marks the switching of the converter and there is no any freedom degree and the control algorithm has not the possibility of changing for instance the order of the switching configurations in the switching sequence. So, there is no freedom in order to improve some characteristics of the converter as balancing of DC-link capacitors, harmonic content, load currents ripple etc.

Any designed switching scheme, whether for CSI or CSR, must satisfy a constraint that only two switches can be at the ON state, one connected to the positive DC bus while the other is connected to the negative DC bus. Connecting two inverters in parallel and under the mentioned constraint, 81 switching states are feasible to form the reference vector. The dwell time of each vector is calculated to satisfy two constraints:

\[
\frac{T_a}{T_o} + \frac{T_b}{T_b} + \frac{T_c}{T_c} = T_{ref}
\]

\[
T_a + T_b + T_c = T_s
\]

In which Ia, Ib, Ic are the three chosen adjacent vectors, Ta, Tb, Tc are the dwell times for each vector and Ts is the sampling time. Since more than one switching state is available for Zero, Small and Medium vectors, it is of significance to design the most proper switching sequence which brings the identical switching sequence in both inverters. In addition, to produce a lower switching frequency and minimize the switching loss, the switching sequence must satisfy the constraint that the transient from one vector to another involves mostly one device switch-ON and one device switch-OFF at each inverter.

### IV. DC Current Balance Control

However significant merits of multi-level converters bring acceptable and practical energy conversion systems to industry, there are some disadvantages which are in need to investigate more and be counted on research. One of the practical drawbacks of some multi-level current source converters is circulating current. The circulating current will lead to generating current harmonics and higher current distortion. In addition, the circulating current increases total loss of the system and it leads to unequal power division between converters which is waste of investment and technology. Generally, the overall system performance decline is the result of circulating current.

The main reasons lead to generating circulating current are:

1. Different pulse width modulation techniques or asynchronous switching strategies.
2. Variations in the time delay of the gating signals of the two inverters, which affects both transient and steady-state current balance. Different circuit parameters, especially manufacturing tolerance in dc-choke parameters.
3. Unequal ON-state voltages of the semiconductor devices, which affects steady-state dc current balance.

The circulating current is mainly consists of zero-sequence components. The total impedance within the zero-sequence circuit of parallel inverter systems with common DC source is very small, and large zero-sequence currents will be circulating in the zero-sequence circuit. The traditional methods to avoid circulating current is using independent and separate AC or DC power supplies or using a transformer in AC side of parallel converters. Applying either solution, being higher in size, mass...
and investment costs are certain. Another traditional solution is adding a phase reactor to configuration. Since, the reactors have lower impedance in lower frequency low-frequency circulating current is not attenuated. Today, using SVM modulation method without Zero vectors is used to eliminate the impact of circulating current. Besides, some d-q axis nonlinear control strategies are introduced to limit the zero sequence circulating current [8-9]. Generally, Elimination of circulating current is one of the most important aspects of multi-level CSI design. One of the features of the introduced switching modulation is DC link current balance control, which results in circulating current minimization.

Synthesizing Medium vectors, two switching states are available for each vector. The Medium vectors located in even sectors affect the magnitude of the positive DC bus currents. On the other hand, the Medium vectors belonging to odd sectors affect the magnitude of the negative DC bus currents. In addition, for each Medium vector, one switching state can make the DC current increase while the other can make the same current decrease.

V. Matlab/Simulink Modeling & Simulation Results

Here the simulation is carried out by seven cases

- 5-Level Parallel Current Source Multilevel Inverter.
- 7-Level Parallel Current Source Multilevel Inverter.

Case 1) 5-Level Parallel Current Source Multilevel Inverter:

Fig. 6: Matlab/Simulink Model of 5-Level Parallel Current Source Multilevel Inverter

Fig. 7 shows the 5 level multilevel inverter current for the proposed 5 level current source multilevel inverter.

Fig. 8: Positive Bus

Fig. 9: Negative Bus

Fig. 8, 9 shows the DC Link Current without and with Current Balance Control

Fig. 10. THD of Output Current Without Filter
Case 2) 7-Level Parallel Current Source Multilevel Inverter:

Fig. 10, 11 shows the THD response of output current without filter and with filter, then the values are 27.35% and 0.58%

Fig. 11: THD of Output Current With Filter

Fig. 12: Matlab/Simulink Model of 7-Level Parallel Current Source Multilevel Inverter

Fig. 13: Inverter’s Output Current

Fig. 14: Positive Bus

Fig. 15: Negative Bus

Fig 14, 15, DC Link Current without and with Current Balance Control

Fig. 16: THD of Output Current Without Filter
As above Fig. 16, 17 shows that, whenever our inverter levels increases, we get pure sinusoidal waveform as well as harmonic free response, we get 24.30% without filter and 0.46% with filter. Here Table I shows the THD Comparisons.

Table 2: THD Comparisons

<table>
<thead>
<tr>
<th>No. of Levels (THD)</th>
<th>Without Filter</th>
<th>With Filter</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Level</td>
<td>27.37%</td>
<td>0.58%</td>
</tr>
<tr>
<td>7 Level</td>
<td>24.30%</td>
<td>0.46%</td>
</tr>
</tbody>
</table>

VI. Conclusion

The new SVM method is proposed in which the switching states are chosen to synthesize the rotating reference current to produce 5-level & 7-level AC current. Novel DC current balance control is proposed. The method employs Medium vectors to eliminate unbalance DC link current. The simulation results validate the proposed method. Generally, the proposed method produces a low level of distortion for practical loading conditions. At high modulation index ma the THD content of the switching current is almost half in comparison to the same current of single-level. As levels increases our THD value decreases, as per IEEE standards the THD value is less than 5% ie., harmonic free response, In this paper THD value for without filter 5 level is 27.37% and 7 level is 24.30% with filter 5-level is 0.58% and 7-level for 0.46%.

References


Mr. M.Vamsi Sree received the Bachelor of Engineering degree in Electrical & Electronics Engineering from BVCE, Amalapuram from JNTU Kakinada in 2008. Currently he is pursuing master of technology in Sri Vasavi Engineering College, Tadepalligudem, A.P. His areas of interests are in Power Systems, Power Electronics and FACTS.

Mr. M.RAMAPRASAD REDDY received the Bachelor of Engineering degree in Electrical & Electronics Engineering from Karnatak University of Dharwad in 1999 and Master’s degree from JNTU Kakinada in 2007. He is presently pursuing Doctoral degree from JNTU, Hyderabad. Currently, working as an Associate Professor in Sri Vasavi Engineering College, Tadepalligudem, A.P. His areas of interests are in power systems, Power electronic control of drives.
Mr. Ch. Rambabu received the Bachelor of Engineering degree in Electrical & Electronics Engineering from Madras University, in 2000 and Master’s degree from JNTU Anantapur in 2005. He is a research student of JNTU Kakinada. Currently, he is an Associate Professor at Sri Vasavi Engineering College. His interests are in power system control, Power Electronics and FACTS.