Implementation of Ultra Low Power 8-Bit CLA and 8-bit ALU CSA Using Single Phase Adiabatic Dynamic Logic

[1]Sweta Mudliar, [2]S. Vasu Krishna, [3]Dr. Sanath Kumar
[1]VLSI System Design, Nalla Malla Reddy Engg. College, Ghatkesar, Hyderabad, AP, India
[2]Dept. of ECE, Nalla Malla Reddy Engg. College, Ghatkesar, Hyderabad, AP, India
[3]Central Institute of Tool Design, Balanagar, Hyderabad, AP, India

Abstract
The paper presents the implementation of ultra low power 8-Bit Carry look-ahead adder and 8-Bit ALU-Carry Select Adder circuit operated by Single-Phase Adiabatic Dynamic Logic (SPADL) which, unlike any other existing Adiabatic logic family uses single sinusoidal supply-clock. This not only ensures high energy efficiency, but also simplifies the clock design which would be otherwise more complicated due to the signal synchronization requirement. Static logic resembled characteristics of SPADL logic substantially decreases circuit complexity with improved driving ability and circuit robustness. In TSMC 0.18µm CMOS technology. CADENCE simulations show that SPADL saves 65% to 50% and 30% to 40% of total energy compared to Conventional CMOS and other existing single phase adiabatic logic based 8-Bit ALU Carry Select Adder for a frequency of 1MHz to 100MHz.

Keywords
Single-Phase, Adiabatic Logic, Energy efficiency, CLA, ALU-CSA

I. Introduction

As the semiconductor process has stepped into the deep submicron phase, the transistor counts integrated in a single chip are increasing continuously. Significant reduction of on chip power density, therefore, has received considerable favour. The dynamic switching is accounted the ring leader of the total power dissipation. As a response, over the past decade, though many techniques have been developed to reduce such an unwanted power overhead, yet adiabatic logic becomes the promising alternative. Adiabatic circuits achieve low energy dissipation by restricting the current flow across devices with low voltage drop and by recycling the energy stored on their load capacitance by using a time varying AC supply voltage. Recent years have seen various Energy Recovery Circuits (ERCs) toward adiabatic circuitry for ultra-low power implementation. Most of them require a four-phase or two phase power-clock. Typical examples are four-phase CPAL [1] and two-phase 2N2N2P2D [2], CEPAL [3], GFCAL [4]. In multiphase clocking scheme, implementation of complex control schemes [5-7] distribution of multiple clock phases [3-7], the management of data dependent clock capacitance fluctuations make the multiphase clocking schemes sensitive to clock skew and may severely limit their high frequency performance [8-9]. In contrast to multiphase circuits, single phase adiabatic circuit relies on just one phase of a power clock waveform for low power and synchronization. Simply a sinusoidal signal can be used as a power clock in a single phase adiabatic circuit. This sinusoidal waveform can be generated with higher energy efficiency than trapezoidal waveforms. In order to make adiabatic logic circuits more feasible and practical in VLSI CMOS applications, single phase operation of the circuits would be needed.

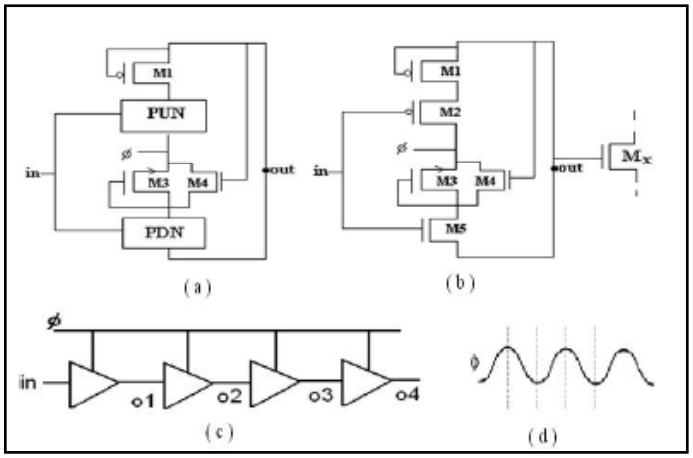

Fig. 1: (a). SPADL General Block, (b). SPADL Inverter, (c) SPADL Inverter Chain, (d). Single Phase Supply Clock

Previously reported SCALD [11] and SCAL [12] circuits use a single-phase power-clock, but the additional reference voltage and current increase the design complexity. Moreover these logic styles are difficult to design due to the optimal value of reference voltage concerning about clock frequency [11-12]. An inverter chain using CAL logic is discussed in [13] with additional timing control clocks to ensure correct operation, resulting in complicated clock tree design and more energy dissipation. Moreover as CAL logic is based on differential signalling, it's higher switching activity reduces energy efficiency. Another typical single-phase ERC family is PAL [16], which is not considered as a real single-phase based ERC since its cascaded circuits need two complementary sinusoidal power clocks. Also PAL [16] logic gates suffer from undesired capacitive couplings, since the output nodes are kept floating instead of zero. Though QAPG [14] has reported as single phase adiabatic logic, yet transistor overheads decrease the energy efficiency. Motivated by the advantages of single phase adiabatic logic the authors have proposed a quasi-static single phase adiabatic dynamic logic (SPADL) [10] recently and also implemented the sequential subsystem. In this paper an 8 bit CLA has implemented by using SPADL logic all the simulations are done by Cadence Spice spectra in TSMC 0.18µm technology and CMOS n-well process and results are compared with some imperative adiabatic logic styles (CAL, QAPG and 2N2N2P2D) including static CMOS also.

II. Overview of SPADL Logic

SPADL requires only one sinusoidal power clock supply, Has simple implementation, and performs better than the Previously proposed diode based logic families [2-4] in terms of energy consumption. SPADL logic features Simplicity and static logic resembled characteristics, which Substantially decreases transistor overheads and the circuit Complexity.

A. Configuration and Operation

Fig. 1(a) and (b) shows the general configuration of SPADL logic block and SPADL inverter. In fig. 1, on basis of applied logic inputs, either pull up or pull down network (PUN or PDN) will be ON at any time instant. The charging and discharging operations of output (out) node of fig. 1(a) can be described as follows:

- When PUN is ON and 'out' is low, if supply clock (φ) ramps up 'out' node will be charged through PUN→M1 by following φ closely and higher logic will be obtained at out node. When φ ramps down, charges will be stored at 'out' node, as they cannot flow back to the supply clock (φ) due to reverse biased M1.
- When PDN is ON and 'out' is high, if φ ramps down, Charge stored at 'out' node flows back to the supply clock (φ) through the PDN→M3and M4.
- When PUN is ON and 'out' is high, if φ ramps up 'out' node will not transit for that clock period. So voltage level of 'out' node will not vary.
- When PDN is ON and 'out' is low, 'out' node voltage will not transit for that complete clock cycle. Hence

$$V(1) = (\varphi|_{max} - |V_{TP}|)$$

$$V(0) = \Delta V \quad (1)$$

Where ΔV is proportional to f (Rd). Rd is the discharging path resistance. As discharging path consists of parallel combination of M3 and M4, Rd will be very low, which improves the lower swing.

Also due to finite voltage drop across M5, gate to source voltage swing of M4 increases. ON resistance (R_d) of a NMOS can be expressed as

$$Rd \propto (VGS-VT)^{-1} \quad (2)$$

So increased gate to source swing reduces the ON Resistance of M4.The output wave forms are shown in fig. 2.

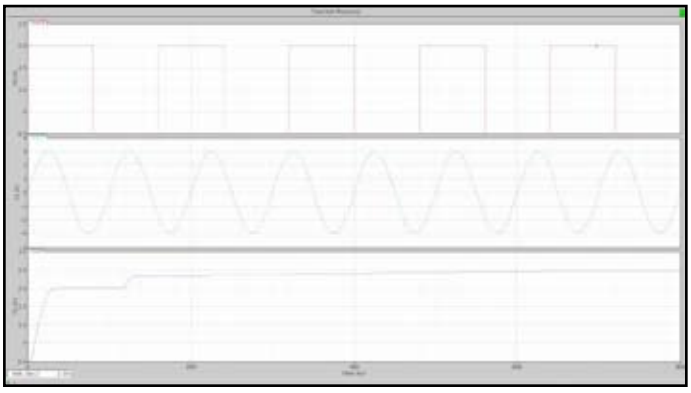

Fig. 2: Output Waveform of SPADL Inverter

Fig. 3, illustrates the operation of the SPADL inverter circuit. Assuming the applied inputs of the circuit areall valid at t=0 time instant. The 1st stage produces its valid-1and valid-0 outputs at t=T/2 time and t=T, respectively. The2nd stage produces its valid-0 output at t=T. Similarly, valid-1outputs of the 2nd and 3rd stages are both produced at t=3T/2, while the valid-0 outputs of the 3rd and 4th stages are both produced at t=2T, and so on. Thus, the total time, Total, needed for data to pass through the 4-stage circuit is 5T/2, where T is the period of Φ. In general, for an N-stage circuit, we have Total= (N+1)T/2. When N >>1, Total = NT/2, which ensures higher speed of SPADL logic. Also in SPADL by using low clock frequency we can drive high frequency input signal.

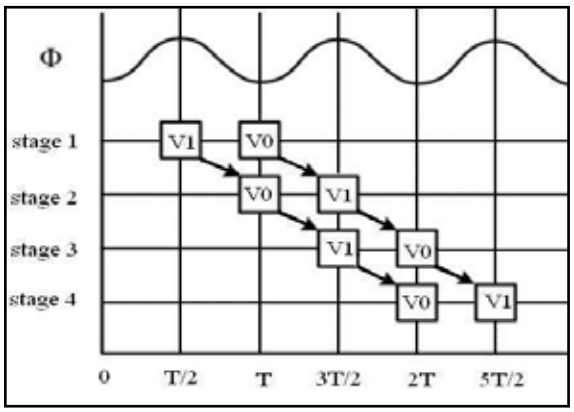

Fig. 3: Operation of SPADL Inverter, V1 and V0 are valid '1' and valid '0' output

B. Energy Consumption of SPADL Logic Circuit

In this section, energy consumption of SPADL logic block, say inverter, are analyzed . From fig. 1, on the basis of input logic level when the supply clock (φ) ramps up (or down) energy dissipation occurs across PMOS diodes (or NMOS diodes) and PUN (or PDN). As PMOS diodes with PUN (or NMOS diodes with PDN n/w) provide the charging (or discharging) path, energy dissipation across diodes can be

Expressed as;

$$E_{Diode} = \int_0^{T1} |V_{TP}|\, i(t)dt$$

$$= \int_0^{C_L(V_{DD}-|V_{TP}|)} |V_{TP}|\, dq$$

$$= [C_L|V_{TP}|\,(V_{DD}-|V_{TP}|)]$$

Where T_1 is the time taken by the supply clock to raise From 0 to VDD, $|^VTP|$ is threshold voltage of PMOS diodes, C_L (= CD1 + CW + CGX) is the output load capacitance. CGX (= βLC_{OX}) is the gate capacitance of next stage NMOS MX. βand L are aspect ratio and length of the channel of MX and COX is the gate oxide capacitance per unit area. C_W is the wiring capacitance. EDiode is independent of operating frequency of supply clock. As clock frequency goes higher, the "diode transistors" have to be sized up proportionately. Moreover threshold voltage drop across PUN and finite ON resistance produce the energy dissipation (E_{Tx}) in charging event and can be shown by the following expression

$$ETx=[½CL|VTP|^2+(RPCL/T)CL(VDD-|VTP|)^2] \quad (4)$$

Therefore for each logic transition total energy dissipation (E Total) in charging path becomes:

$$E\ Total = E_{Diode} + E_{Tx}$$

$$\approx [C_L|V_{TP}|(V_{DD}-|V_{TP}|)] + [½C_L|V_{TP}|^2] \quad (5)$$

(As RC/T<< 1 for moderate fan-out) (8)

During discharging almost same amount of energy dissipates in the discharging path. So the maximum possible energy saving of SPADL logic over CMOS in a full clock cycle is

$$\eta\% = \{ [CL|VTP|(VDD-|VTP|)] + [½CL|VTP|^2] / CLVDD^2\} x100$$

$$\approx 2\alpha\,[1 - \alpha^2/2] \times 100 \text{ where } \alpha = \{|V_{TP}|/V_{DD}\} \quad (6)$$

It is seen that there is no significant improvement in energy efficiencies of SPADL logic by lowering threshold voltage of PMOS and NMOS diode. However to achieve higher integration density or to maintain high drive current, voltage scaling is important. Still we cannot reduce threshold or supply voltage arbitrarily. As aggressive scaling of technology results in different leakage components become a significant issue of total power dissipation

in adiabatic CMOS logic circuit measures proportionately more than is customary. This measurement and others are deliberate, using specifications that anticipate your paper as one part of the entire proceedings, and not as an independent document. Please do not revise any of the current designations.

III. 4-2 Compessor by SPADL Logic

In this section, we first describe SPADL gates, and then we Present the design of adiabatic gates and 4-2 compressor using SPADL logic

A. SPADL Complex Gate Design

Complex gates can be easily implemented by using simple CMOS pull-up and pull-down network. In fig. 1(a), by replacing the PUN (pull up network) or PDN (pull down network) we can implement the AND gate, XOR gate, 2 to 1 MUX with SPADL circuit topology. Fig. 4 shows implementation of all these gates with simple buffer circuit also. Static logic resembled characteristics of SPADL logic Substantially decreases the transistor overheads in complex gate design. In buffer circuit we have modified our logic slightly shown in fig. 4 (d). When Φ ramps up and 'in'=1 (or 0), NMOS (or PMOS) (having gate i/p 'in') is turned ON and 'out' node is charged (or discharged). So we get same logic as 'in' at out node and hence the circuit acts as buffer. Thus Complex gate design can be made very modular and simple. The layouts of SPADL AND, OR, XOR and NOT gates are shown in fig. 5. These layouts are created by using CADENCE suite based on TSMC 0.18µm CMOS n-well process technology. A design rule checking (DRC) and the circuit structure extraction are performed on the layout view of the adiabatic system. Then, the view extracted from the layout and the original schematic view is compared with the Layout Versus Schematic (LVS) tool Layout of SPADL gates are shown in fig. 5.

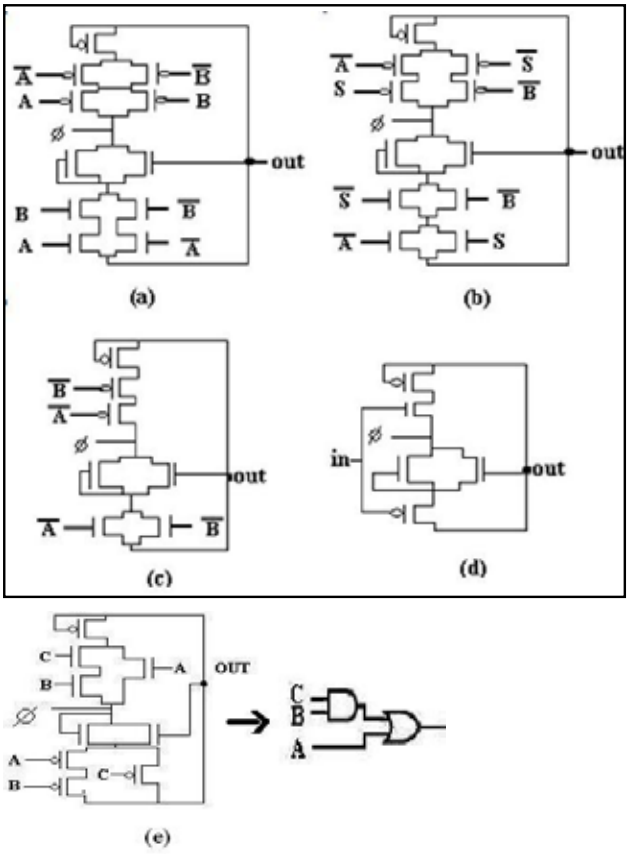

Fig. 4: SPADL Gates (a) XOR, (b). 2 to 1 MUX, (c). AND, (d). buffer, (e). AND_OR having o/p (A+BC)

B. SPADL 8-Bit CLA Implementation

A significant speed improvement in the implementation of a parallel adder was introduced by a Carry-Lookahead-Adder (CLA) developed by Weinberger and Smith in 1958 [9-10].The CLA adder is theoretically one of the fastest schemes used for the addition of two numbers, since the delay to add two numbers depends on the logarithm of the size of the operands: Δ= log[N].

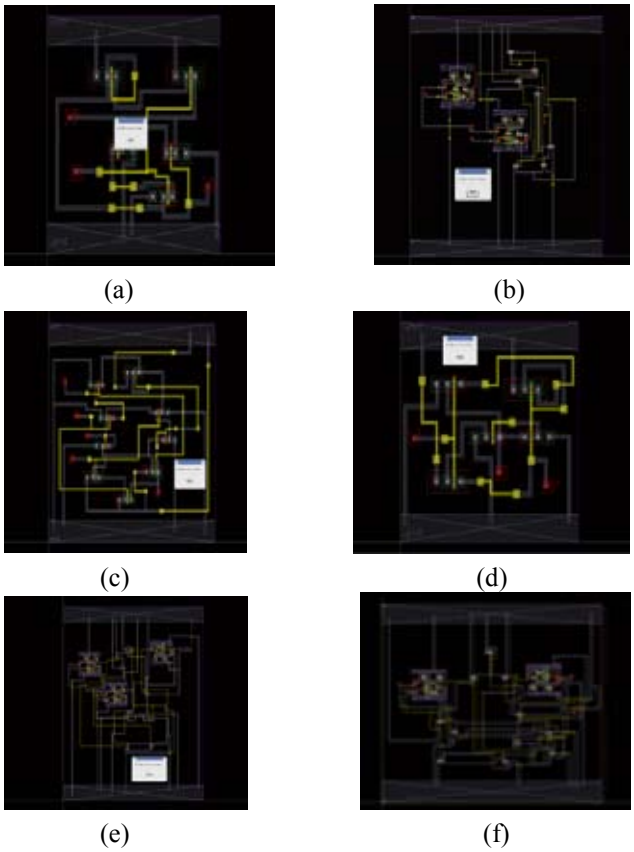

Fig. 5: Layout of SPADL Gates (a) Inverter, (b). AND, (c). AND-OR, (d). Buffer, (e). Mux, (f). XOR

There fore the delay of CLA is not directly proportional to the size of the adder N, but to the number of levels used. This log dependency makes CLA one of the theoretically fastest structures for addition. We have designed and simulated an 8-bit CLA using SPADL, CAL, QAPG, 2N2N2P2D and static CMOS respectively. The simulations are done by CADENCE spice spectra, using TSMC 0.18µm CMOS technology. A 3V peak-to peak sinusoidal voltage supply was used as the power clock Φ throughout our simulation for SPADL logic. The other adiabatic CLAs are simulated under different clocks, provided by the literatures. All the output nodes are loaded by 25 fF capacitors to get more stable waveform.

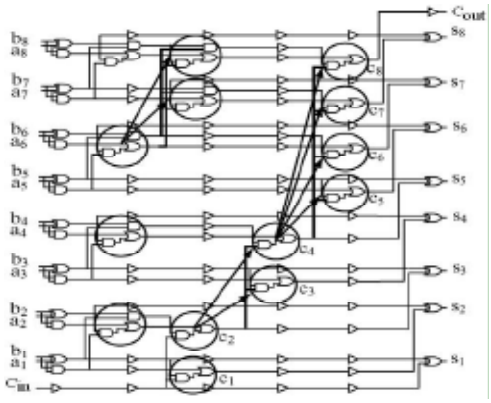

Fig. 6: Schematic of SPADL 8 Bit Carry Look-Ahead Adder Circuit

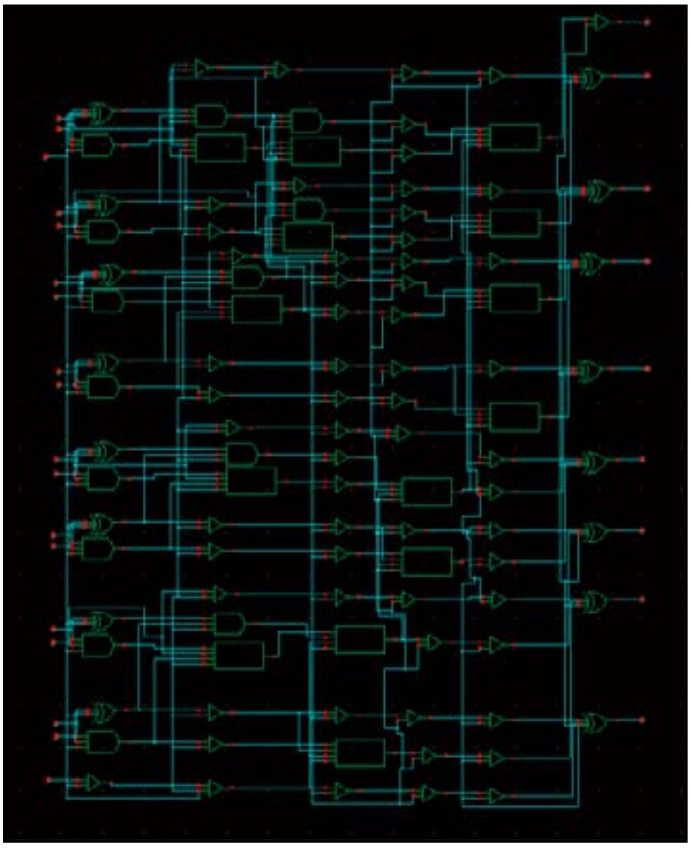

Fig. 7: Virtooso Schematic of SPADL 8 Bit Carry Look-Ahead Adder Circuit

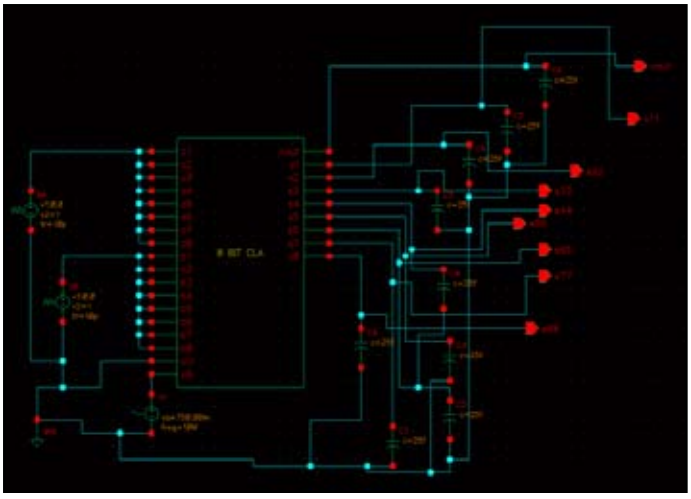

Fig. 8: Virtooso Schematic of SPADL 8 Bit Carry Look-Ahead Adder Circuit Block

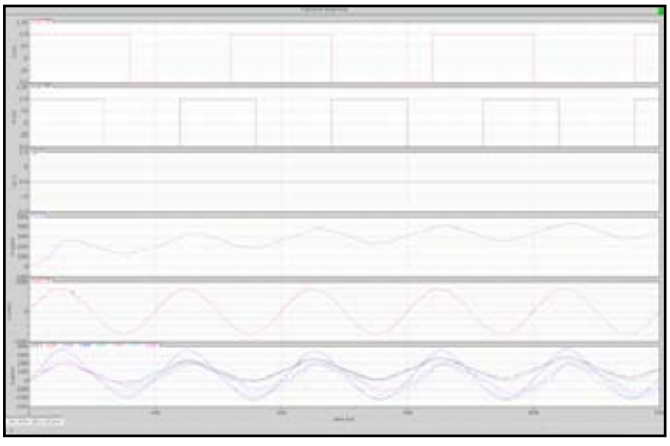

Fig. 9: Output Waveforms of 8-Bit Adiabatic CLA

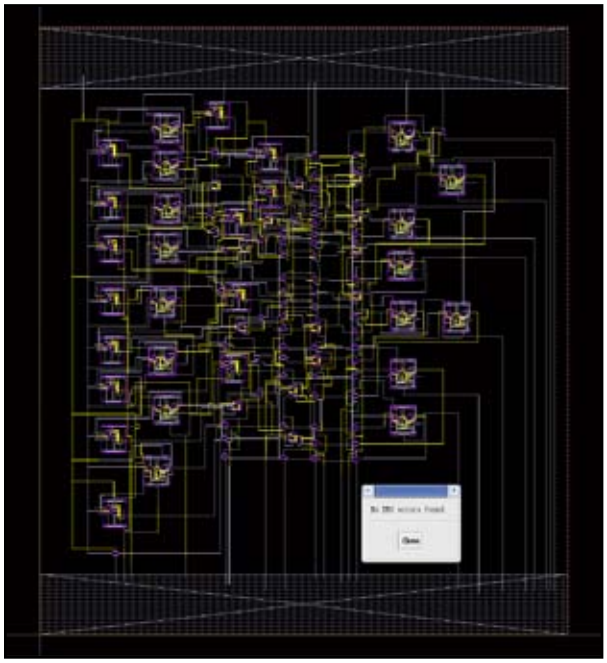

Fig. 8: Layout of 8-Bit Adiabatic CLA

C. SPADL 8-Bit ALU-CSA Implementation

The 8-bit ALU was formed by combining three 4-bit ALU's with 5 multiplexers as shown in fig. 2. The design of the 8-bit ALU is based on the use of a carry select line. The four lowest bits of the input are fed into one of the 4 bit ALU's.

The carry out line from this ALU is used to select the outputs from one of the two remaining ALUs. If carry out is asserted then the ALU with carry in tied true is selected. If carry out is not asserted then the ALU with carry in tied false is selected. The outputs of the selectable ALUs are multiplexed together forming the upper and lower 4 bits, and carry out for the 8 Bit ALU.

IV. Simulation Results and Discussion

The results of the RTL compilation are shown bellow. The results coming from the CADENCE simulation of the SPADL arithmetic units described above are presented and Discussed in this section and different aspects of SPADL logic has been explored due to the simulation. In this section energy dissipation measurements were determined directly from the CADENCE simulations outputs, by integrating the power over the period of oscillation. For the adiabatic circuits we have initially assumed a 100% energy-efficient power- clock generator, in order to compare the Results with the literature.

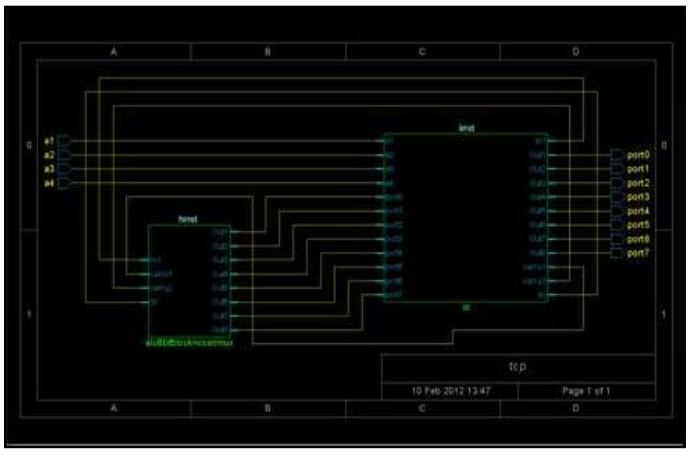

Fig: 9: Top Module Block of RTL 8 BIT ALU CSA

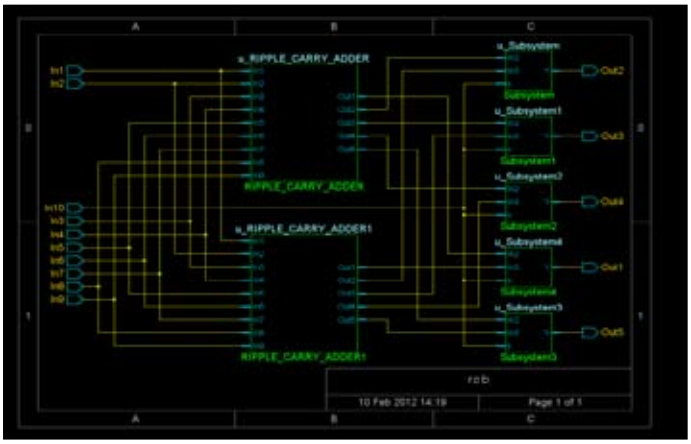

Fig. 10: RTL Schematic Of SPADL ALU-CSA

We take it into our account then SPADL shows better efficiency as it uses energy efficient sinusoidal source, compared to other multiphase clocked logic at low frequency, all single phase logic styles (CAL QAPG and SPADL) promise substantial energy savings compared to static CMOS, with the lowest energy consumption from SPADL. SPADL based compressor consumes only 34% and 52% of total energy consumed by conventional4-2 compressor at 10MHz and 100 MHz frequencies If respectively as diodes using MOS transistors are weak in driving capability, hence in SPADL based ALU_CSA are introduced at the end of 3 stages to improve the driving ability That causes some extra power dissipation. Still at 100 MHz frequency, SPADL logic based compressor consumes only 62% and69% energy of the CAL and QAPG

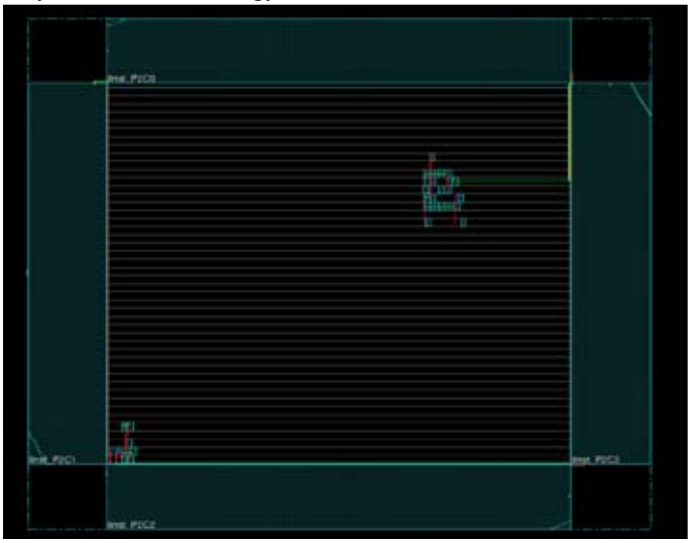

Fig. 10: SOC Schematic Of SPADL ALU-CSA

Operating frequency so much at low frequencies as it is mainly due to the diodes and conventional clocks. As clock frequency goes higher, the "diode transistors" have to be sized up proportionately, which increases the capacitances. The resistive dissipation (which is proportional to RC/T) increases as well. On the other hand, 2N2N2P2D compressor does not show much power savings since 2N2N2P2D logic circuit has floating output node during part of the clock cycle. Simulation shows that this circuit can only work well if there is substantial capacitance to ground. Otherwise, capacitive coupling between the floating output node and clock would cause inadequate operating margins, which is undesirable as the output is directly connected to the input of the next stage logic in 2N2N2P2D.

V. Conclusion

This paper presents the SPADL 8-Bit ALU-CSA circuits using single phase ac power supply. This SPADL logic style can enjoy minimal control overheads and are thus capable of Operating at high speeds, while achieving high-energy efficiency. Compared to other existing single phase based Logic SPADL saves 30% to 40% of total energy for clock frequencies ranging from 1MHz to 100 MHz frequency. High energy efficiency of SPADL makes it suitable for implementing performance efficient VLSI circuitry.

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Sweta Mudliar received her B.E. degree in Electronics and Communication from All Saint's College of Technology Bhopal (M.P) India in 2009, the M.Tech degree in VLSI SYSTEM DESIGN from Nalla Malla Reddy College of Engg, JNTU, Hyderabad, AP, India, in 2012. She was a lecturer, with Department of Electronic and Communication, SIRT College Bhopal (M.P), in 2010. She also having a diploma degree in VLSI and Embedded System Design from CITD Hyderabad, AP, India in 2012.