VHDL based Multiple Traffic Lights Controller

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Abstract
16 bit microprocessor design in VHDL with implementation on CPLD provides compact and robust solution for existing Traffic System. Mechanical traffic lights got degrade after some time due to environmental factors which affects the delay. CPLD based Traffic lights provide programmable accurate delay with preventive measures from environmental hazards. With VHDL based traffic lights controller we can also control multiple locations at a same time.

Keywords
CPLD,Xilinx.

I. Introduction

Traditionally traffic lights are controlled by microcontroller 89C51. The primitive mechanical traffic lights have no way of having a versatile delay. But using CPLD as a 16-bit µP and use it in the domestic application to improve the primitive mechanical traffic lights.
This project attempts control the traffic lights using VHDL. Being an electronic system it is reliable, compact and maintenance free. VHDL makes the system versatile as the on off times can be easily varied by changing the delay loops through software. Even the sequence of lights i.e. whether the yellow light has to glow or not can be programmed easily by modifying the software.
This project is practically implemented and tested. Because Programmable Integrated Circuits provides repeatability and flexibility, we can program it more than 10,000 times. And this is not possible is fixed logic IC's.
The best part of using CPLD is we can easily reprogram it. We do not have need to remove the CPLD from the hardware we can program it by placing it into the same board.

A. Functional Block Design

It includes:

- CPLD XC9572
- Clock Generator(Astable Multivibrator)
- ULN2803 Driver
- Traffic Lights
- Power Supply(+5V,+12V)

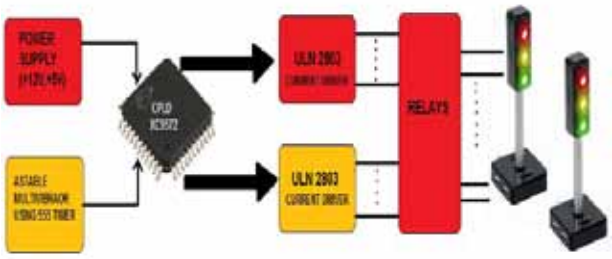


Fig 1: Block Diagram

CPLD XC9572 In the world of digital electronic systems, there are three basic kinds of devices: memory, microprocessors, and logic devices. Memory devices store random information such as the contents of a spreadsheet or database. Microprocessors execute software instructions to perform a wide variety of tasks such as running a word processing program or video game. Logic devices provide specific functions, including device-to-device interfacing, data communication, signal processing, data display, timing and control operations, and almost every other function a system must perform. In case of CPLD, it has wiring among the logic in the IC. So, the wiring on the printed board can be made little.

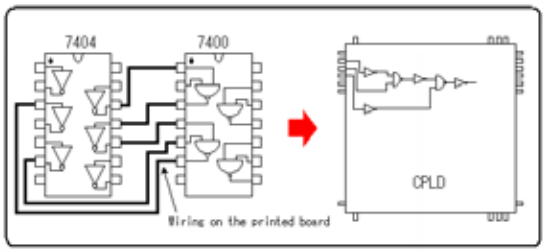


Fig. 2: architecture of CPLD

Parts name	Number of pins	Specification
XC9536-15PC44C	44pin PLCC	2FB/36macrocells/800gates
XC9572-15PC44C	44pin PLCC	4FB/72macrocells/1600gates
XC9572-15PC84C	84pin PLCC	4FB/72macrocells/1600gates
XC95108-15PC84C	84pin PLCC	6FB/108macrocells/2400gates

PLCC : Plastic Leaded Chip Carrier
FB : Function Block

Fig. 3: Different CPLD specifications

Complex Programmable Logic Devices (CPLDs) are exactly what they claim to be. Essentially they are designed to appear just like a large number of PALs in a single chip, connected to each other through a cross point switch They use the same development tools and programmers, and are based on the same technologies, but they can handle much more complex logic and more of it.
Xilinx is a vendor of CPLD products and manufactures a family known as the XC9500. Logic blocks, or function blocks in Xilinx's terminology, each contain 18 macrocells, the outputs of which feed back into the switch matrix and drive I/O pins as well. XC9500 CPLDs contain multiples of 18 macrocells in densities from 36 to 288 macrocells. Each function block gets 54 input terms from the switch matrix. These input terms can be any combination of I/O pin inputs and feedback terms from other function blocks macrocells.

B. Traffic Lights

A traffic signal, controls vehicle traffic passing through the intersection of two or more roadways by giving a visual indication to drivers when to proceed, when to slow, and when to stop. In some cases, traffic signals also indicate to drivers when they may make a turn. These signals may be operated manually or by a simple timer which allows traffic to flow on one roadway for a fixed period of time, and then on the other road-way for another fixed period of time before repeating the cycle. Other signals may be operated by sophisticated electronic controllers that sense the time of day and flow of traffic to continually

adjust the sequence of operation of the signals. We can control multiple traffic lights of different roads by using single CPLD chip. It reduces the cost of the project.

C. Clock Generator

555 timer operates in modified astable multivibrator generating clock of 4MHz provides clock cycles to execute instructions of program load into CPLD.

D. ULN2803 Driver

ULN28xx high voltage, high-current Darlington arrays are ideally suited for interfacing between low-level logic circuitry and multiple peripheral power loads. Typical power loads totaling over 260 W (350 mA x 8, 95 V)

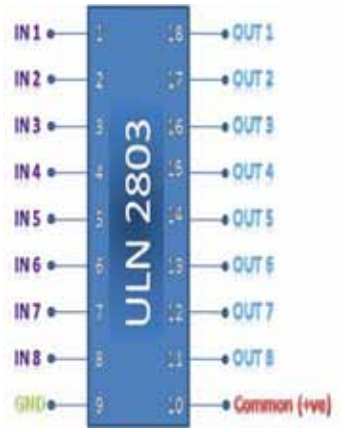


Fig. 4: Pin Diagram

can be controlled at an appropriate duty cycle depending on ambient temperature and number of drivers turned ON simultaneously. Typical loads include relays, solenoids, stepping motors, magnetic print hammers, multiplexed LED and incandescent displays, and heaters.

II. Working

Traffic lights operate with the rising edge of the clock. This is generated by using the 555 timer (Astable Multivibrator).The Programming is done in VHDL language. Its working is similar to Normal traffic lights. But single CPLD chip can be used to control the traffic of number of road signals. Because it has large number of input and output pins . in its working +5V is given to the CPLD and as it receive the rising edge of clock, and it starts its sequence of traffic lights. We can increase or decrease the delay between the

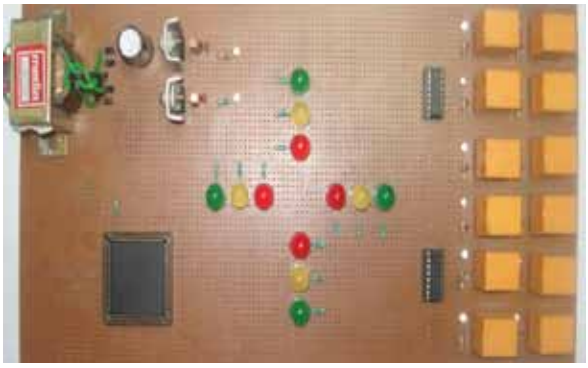


Fig. 5: Practical Implementation

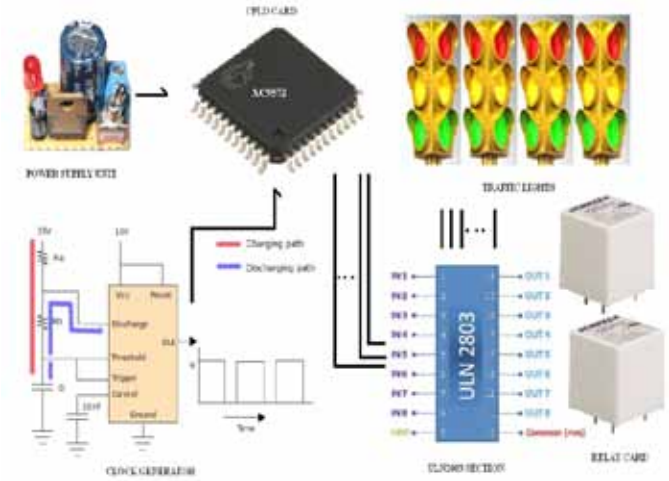


Fig. 6: logical diagram of VHDL based 16-bit µP for Traffic Light Controller

transition of signals according to the requirement. It reduces the complexity and have number of advantages of using CPLD instead of microcontroller. LED's are connected to CPLD pins through ULN2803(current driver) and Relays. The logic which will be one of the pin will be given to current driver. Current driver will invert the logic and will give this invert signal to the relay and the logic which will be High it will activate the coil and hence on the light and vice versa.+12 v supply is given to Relays.

Relays are connected to zener diode to ULN2803 to avoid the back off current

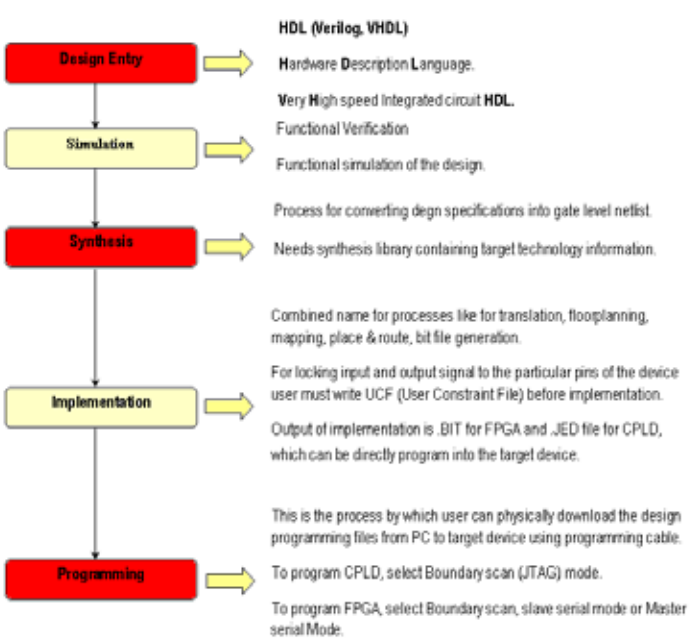


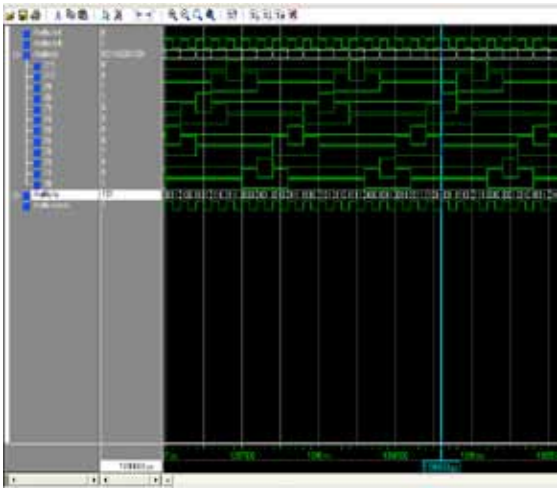
Fig. 7: design Steps

VHDL Programming

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

entity traffic is
port(clk,rst:in std_logic;
c:out std_logic_vector(0 to 11));
```

```
end traffic;
architecture Behavioral of traffic is
        signal a:std_logic_vector(0 to 2):="000";
        signal clock:std_logic:='0';
begin
process(clk,rst)
variable d :integer:=0;
 --variable clock :std_logic;
begin
if clk'event and clk='1' then
```



```
d:=d + 1;
        if d=1000000 then
                clock<=not clock;
                d:=0;
                end if;
                end if;
                end process;
                process(clock,rst)
        begin

        if (rst='0'and  rising_edge(clock))
        then
        if rst='1' then
        c<="000000000000";
        end if;
        a<=a + "001";
if(a="000")then
         c<="001001001100";
        end if;
        if(a="001")then
         c<="001001010010";
        end if;
        if(a="010")then
         c<="001001100001";
        end if;
        if(a="011")then
         c<="001010010001";
        end if;
        if(a="100")then
         c<="001100001001";
        end if;
        if(a="101")then
         c<="010010001001";
        end if;
        if(a="110")then
         c<="100001001001";
        end if;
        if(a="111")then
         c<="010001001010";
        end if;
        end if;
        end process;
        end Behavioral;
```

A. Simulation

Fig 7:Simulation on MODEL SIM

B. Pin Assignemnt

Table 1 : Pin Assignment

Sr. No.	Pin Description	Pin No.
54	SW1	84
55	SW2	1
56	SW3	2
57	SW4	3
58	GCK1	10
59	GCK2	12
60	RELAY1	17
61	RELAY2	15
62	GEN0	4
63	GEN1	5
64	GEN2	6
65	GEN3	7
66	GEN4	11
67	GEN5	13
68	GEN6	14

C. Results

HDL Synthesis Report
Macro Statistics
ROMs : 1
8x12-bit ROM : 1
Adders/Subtractors : 1
32-bit adder : 1
Counters : 2
3-bit up counter : 1
32-bit up counter : 1
Registers : 2
1-bit register : 1
12-bit register : 1

Fig. 9: Report on xilinx

Advanced HDL Synthesis Report
Macro Statistics
ROMs : 1
8x12-bit ROM : 1
Adders/Subtractors : 1
32-bit adder : 1
Counters : 2
3-bit up counter : 1
32-bit up counter : 1
Registers : 13
Flip-Flops : 13

Cell Usage :
BELS : 211
AND2 : 73
AND3 : 3
AND4 : 4
AND8 : 4
INV : 70
OR2 : 22
XOR2 : 35
FlipFlops/Latches : 48
FD : 48
IO Buffers : 14
IBUF : 2
OBUF 12

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