# Review Paper on Comparison between 40nm n-channel Double Gate and TRI-GATE MOSFET

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**Abstract**
MOSFET is the most important device in modern high-density advanced Integrated Circuits (IC). Since 1970 the gate length of MOSFETs in production ICs has been scaled down at a rate about 13% per year, and it will continue to shrink in the foreseeable future. The reduction of device dimensions is driven by requirements for both performance and density. The physical dimensions of bulk MOSFETs have been aggressively scaled down and these conventional devices will soon be experiencing limited improvements due to the scaling down. In order to continue performance improvements, new device architectures are needed. As the scaling of MOSFET into sub-40nm regime, DG-MOSFET and TG-MOSFET have replaced traditional bulk MOSFET. This paper comprises the variations in threshold voltage of 40nm DG-MOSFET and TG- MOSFET by using different Doping profiles, variation in the Biasing voltages, variation in the gate material, variation in gate oxide thickness, sub-threshold swing, $I_{on}/I_{off}$ ratio and Drain Induced Barrier Lowering (DIBL).

**Keywords**
Threshold Voltage ($V_{th}$), DIBL, $I_{on}/I_{off}$ Ratio, Subthreshold Swing, Trans-conduction, Static Power Consumption.

## I. Introduction

Recent progress to scale down the transistors to smaller dimensions provides the faster transistors, as well as lowers the effective density in terms of transistors area. The transistor scaling necessitates the integration of new device structures. The Double-Gate (DG) and Tri-Gate (TG) MOSFETs are example of this, which are capable for nanoscale integrated circuits due to their enhanced scalability, compared to the bulk or Si-CMOS.

The Multi-Gate is definitely wise choice in place of BULK MOSFETs. In DG MOSFET both the gates are placed in symmetry covering the channel which are present at the opposite of each other. The channel is formed near the gate. In this device both the gates are connected to the same potential and they have the same dimensions so it is known as symmetric DG-MOSFET.

The Multi-Gate transistor is considered one of the most promising devices for extremely scaled CMOS technology generations. Indeed, due to a good electrostatic control of the channel by the two gates, it is expected to provide smaller short-channel effects (SCE), near ideal sub-threshold slopes and higher drive currents when compared to single-gate (SG) transistors.

Controlling the channel by multiple (i.e. double, triple, surround, etc.) gates has its supremacy of better control over the channel inversion, so the short channel effect is reduced. More specifically, reducing the current leakage and eliminating the drain-induced barrier lowering (DIBL) effect.

## II. Device Structure and Specification

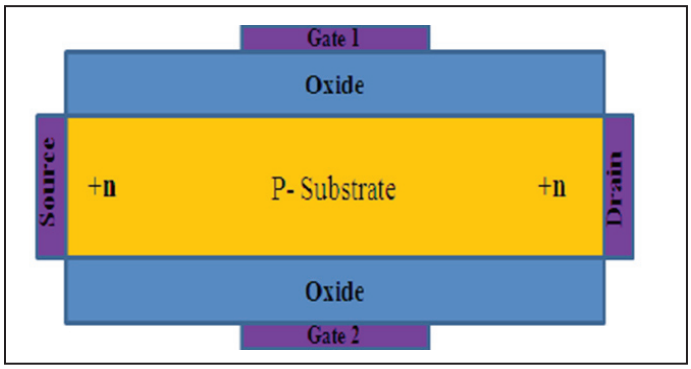


Fig 1: Structure of n Channel DG MOSFET

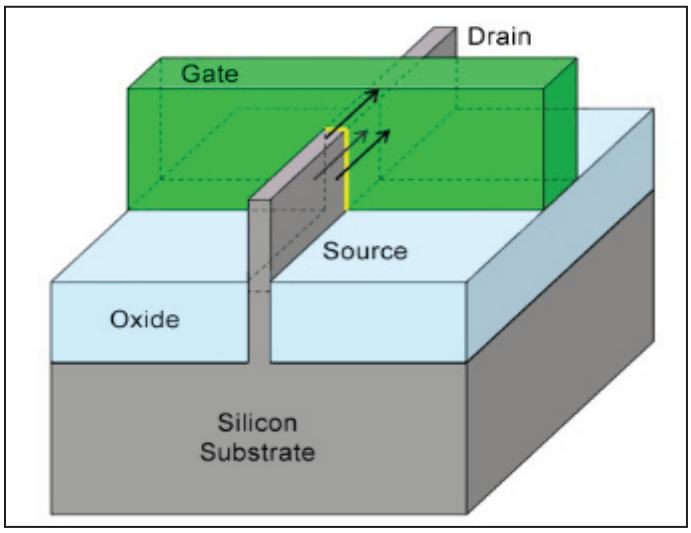


Fig. 2: Structure of n-channel Tri-Gate MOSFET

## III. Comparison

Here is the comparison between the different parameters of Double-Gate MOSFET and Tri-Gate MOSFET.

### A. Variation in Threshold Voltage (VT)

One of the most important parameters of the MOSFET is the threshold voltage. The ideal threshold voltage is given in Eq. (1). However, when we incorporate the effects of the fixed-oxide charge and the difference in work function, there is a flat-band voltage shift. Additionally, substrate bias can also influence the threshold voltage. When a reverse bias is applied between the substrate and the source, the depletion region is widened and the threshold voltage required to achieve inversion must be increased to accommodate the larger Qsc. These factors in turn cause a change in the threshold voltage:

$$V_T \approx V_{FB} + 2\psi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\psi_B + V_{BS})}}{C_o}, \quad \text{Eq. (1)}$$

where $V_{BS}$ is the reverse substrate-source bias.

Factors determining Threshold Voltage:

### 1. Impact of Doping Profile in $V_{th}$

Increasing doping concentration threshold voltage also increases. Therefore, we can better control the threshold voltage by varying the doping concentration of the channel. In our present work, we have examined the effect of doping concentration on Threshold voltage of Double-Gate MOSFET and Tri-Gate MOSFET. Impact of doping concentration in Vth is more in Tri-Gate as compared to Double –Gate MOSFET.

### 2. Impact of oxide($SiO_2$) Thickness in $V_{th}$

In MOSFET, there are three terminals such as source (S), drain (D) and gate (G). The top layer of the MOS system is the metal, and it is used to form the gate electrode. Central to the functionality is the thin insulating layer, the gate-oxide. Gate oxide layer or known as dielectric is to provide an isolation layer between metal and semiconductor so that there is no current flow between gate and substrate of the semiconductor. With the variation in oxide thickness Threshold voltage of the MOSFET changed significantly. This variation is more in Tri-Gate MOSFET as compared to Double-Gate MOSFET.

### 3. Impact of Gate Material in $V_{th}$

Threshold voltage of the MOSFET inversion layer is correlated with the work-function difference between the gate and the channel. Using metal would result in a higher Vt as compared to poly-silicon.

### 4. Impact of Biasing Voltage in $V_{th}$

The body bias circuit technique can dynamically modify the threshold voltage during circuit operation. The threshold voltage can be increased or decreased depending upon the polarity of the voltage difference between the source and the body terminal.

### 5. Impact of channel Thickness in $V_{th}$

Channel thickness also play significant role in decreasing and increasing the Threshold voltage of the MOSFET.

### 6. Impact of oxide material in $V_{th}$

In Tri-Gate MOSFET Gate coupling is from three sides of the substrate due to this Threshold voltage of Tri-Gate is low as compared to Double-Gate MOSFET.

### B. Variation in Drain Induced Barrier Lowering (DIBL)

DIBL is caused by the encroachment of the depletion region from the drain into the channel. At high drain bias, the depletion region strongly affects the channel potential. As a result, the threshold condition can be reached at a lower gate voltage since the drain has already created a large portion of the depletion region. Strong DIBL is an indication of poor short channel behavior. However, since the transistor is not operated at a lower drain bias, DIBL itself is not a parameter that is directly related to circuit operation, but rather it is an indication of the degraded device characteristics.

As we scale down channel length of MOSFET. It reduces the Gate coupling with the channel which increases DIBL in the subthreshold region (weak inversion). For reducing DIBL we decrease Drain voltage which further reduces Drain current which is insignificant. However, at shorter lengths the slope of the current vs. gate bias curve is reduced, that is, it requires a larger change in gate bias to effect the same change in drain current. So we find some alternate methods for reducing DIBL. Which are altering the MOSFET structure i.e. Double–Gate MOSFET and Tri-Gate MOSFET. DIBL is low in Tri-gate as compared to Double-gate MOSFET

### C. Variation in Sub-threshold Swing (SS)

Sub-threshold swing is defined below threshold voltage as the voltage change required changing the current decade times. Sub threshold is the swing generated by the drain current when the gate voltage is varied or increased from zero to the threshold voltage. The fluctuation in drain current is measured in mv/decade and the x-axis is the channel length in nm. The swing in DG MOSFET is lower than SOI MOSFET and which ideal characteristics for MOSFET. For ideal transistor the drain current should be zero up to the threshold voltage. So, we can conclude that DG MOSFET successfully removes the sub threshold swing.
Tri-Gate MOSFET has less Sub-threshold Swing as compared to the Double-Gate MOSFET.

### D. Variation in $I_{on}$/ $I_{off}$ ratio

$I_{on}/I_{off}$ is the figure of merit for having high performance (more Ion) and low leakage power (less $I_{off}$) for the CMOS transistors. Typically, more gate control leads to more $I_{on}/I_{off}$. Trigate MOSFET has more gate control because gate control is from three sides that's the reason that Trigate has more $I_{on}/I_{off}$ ratio as compare to Double gate MOSFET.

## IV. Conclusion

In this Review Paper Double Gate and Tri Gate modelling styles of MOSFET were discussed. Variation in threshold voltage (Vm), SS DIBL $I_{on}/I_{off}$ have been compared for Double gate MOSFET and Tri-gate MOSFET. Tri-gate bulk MOSFET have higher threshold voltage, lower subthreshold swing, drain induced barrier and more Ion/Ioff ratio as compared to Double Gate MOSFET. Thus it appears to be promising device architecture for transistor scaling to the end of the technology roadmap.

Table 1: Comparison on Different Parameters of DG MOSFET and TG MOSFET

| S. No. | Design | $V_{th}$ | DIBL | SS | $I_{on}/I_{off}$ Ratio |
|---|---|---|---|---|---|
| 1. | DG MOSFET | Low | High | High | Low |
| 2. | TG MOSFET | High | Low | Low | High |

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