

Folding & Interpolating ADC using Low Power Folding Amplifier

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Abstract

Folding and interpolating A/D converters have been shown to be an effective means of digitization of high bandwidth signals at intermediate resolution. The paper focuses on design of folding & interpolating ADC using low power folding amplifier. The folding amplifier can be used to produce more than one zero-crossing point to reduce required number of comparators. The converter architecture is designed with reduced number of comparators and minimum hardware. To achieve the design goal, folding amplifier is used in the design of coarse and fine converter both. To reduce the power consumption, encoder based on XOR-OR logic is used. The design is implemented using 0.35 μ m technology at 3.3V.

Keywords

Comparator, Encoder, Folding Amplifier, Folding & Interpolating ADC, Interpolation, Low Power.

I. Introduction

Flash ADC has the highest conversion rate because of its fully parallel architecture. However, an N-bit flash ADC needs $2^N - 1$ comparators, which consume large power and occupy area [1, 8]. Folding architecture is an alternative approach to reduce the complexity of flash ADC and still keep high conversion rate [2]. Before the outputs of the preamps are fed into comparators, folding amplifiers are inserted. Folding amplifier combines the outputs of several preamplifiers and generates folding waveforms, which contains information of those preamplifiers. After folding processing, one comparator deals with more quantization levels. Hence, the number of the comparators is reduced. The number of comparators required for a folding ADC decreases as the folding order increases. The architecture still keeps high-speed potential [6, 7].

Another attractive feature of folding and interpolating ADC is that high-speed sample and hold amplifier is optional due to parallel operation of fine & coarse converter. However, in most of the papers coarse converter is similar to flash ADC. Liu et al proposed design of coarse converter using folding circuit similar to fine converter [10]. Wenzek suggested cascaded dummy differential amplifiers with similar structure like those in the folding stage of the fine converter to overcome the different latencies of coarse and fine converter [11].

The main focus over here is to design Folding & Interpolation ADC for medium resolution applications with minimum comparators and hardware. Section-II discusses folding & interpolating design with brief overview of the folding operation. The architecture of Folding & Interpolating ADC with system level design considerations is discussed in section-III. The details of implemented folding amplifiers are shown in Section-IV. Section-V discusses interpolation technique. The low power comparator is described in Section-VI. Finally, with simulation results, performance of the converter design is verified.

II. Folding & Interpolating ADC

The concept of Folding A/D converter was first introduced by Arbel and Kurz [9] in 1975. The main motivation was the dramatic reduction of the number of comparators required in the design. Fig. 1 shows the block diagram of a folding A/D converter. The folding and interpolating A/D converter contains two separate converters, namely, the coarse and the fine converter. The input signal is fed into both converters in parallel. The input voltage is applied to a pre-processing circuit depicted as the "folding circuit," and the output of this folding circuit is connected to a N-n-bits fine A/D converter. The input signal is also directly connected to a n-bits coarse A/D converter.

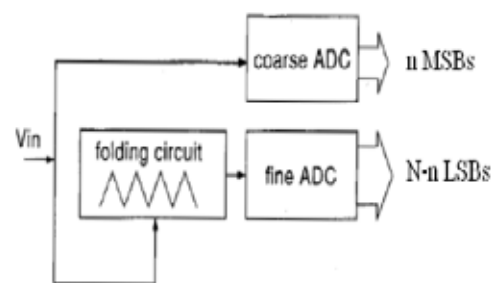


Fig. 1: Block Diagram of folding ADC

III. Architecture of Folding & Interpolating ADC

In Folding & Interpolating ADC, number of zero-crossing points Z is determined by the following equation

$$Z = N_F \cdot F_F \cdot I \dots\dots\dots (1)$$

where N_F is the number of primary folding waveform, F_F is the folding factor and I is the interpolating rate.

The choice of folding factor F_F and number of folding block

N_F play very important role in design of Folding ADC. The speed and the bandwidth of the ADC are affected by the bandwidth of the folding circuits. Moreover, the accuracy of the A/D converter is dominated by the folding circuits in which the correct zero crossing points must be generated to meet the required resolution. In order to achieve low power consumption, low input capacitance & small chip area, number of parallel folders should be reduced and folding factor should be increased. Also by choosing higher number of parallel folders, complexity of hardware increases. Here, zero crossing points are generated to achieve high speed, accuracy and low power operation.

The aim of the fine converter inside the folding and interpolating A/D converter is to process the input signal, either a sampled or an unsampled signal, and to resolve it into the lower significant bits of the word length of the whole analog-to-digital converter. The output signals of the fine converter are then synchronized with output signals of the coarse converter and combined

to yield the output of the complete converter. Using such arrangement can reduce the number of needed comparators immensely, when compared with the flash A/D converter. The fine converter is composed of a folding stage, an interpolation stage, a comparator stage, and an encoder as shown in fig. 2.

Fig. 2 shows block diagram of implemented 6-bit folding & interpolating converter. Total 64 zero crossing points are obtained by selecting folding factor $F_F=8$, Interpolating Factor=2 and Number of Folding block=4. The Fine converter

uses folding amplifier with folding factor $F_F=8$. The encoder generates four fine bits while 2 coarse bits are generated using

folding amplifier with folding factor $F_F=4$ and $F_F=2$.

The implemented architecture offers many advantages.

In most of the designs fine converter uses 2^n number of comparators, where n is the number of fine bits and coarse

converter uses $2^m - 1$ number of converter, where m is the number of coarse bits. In this architecture, cyclic thermometer code is converted into binary using XOR-OR Encoder, due to which the number of comparators required are only 8 (equal to number of folded signals + number of interpolated signals). Instead of using Flash ADC for coarse converter design, folding circuit is used. This helps in reducing number of comparators. As resolution is small, the saving in number of comparators is not large. However, this helps in reducing latency of two converters at the cost of two additional folding amplifiers. Further, input to all the comparators are differential signal (output of folding stage), which makes comparator less sensitive to noise and offset. Because comparator only take decisions about zero crossings, in accurate gain and offset errors of preamplifier appear as INL rather DNL. In this architecture, coarse bits are obtained without use of any encoding stage. Also the folding amplifier, comparators and encoder blocks are designed to achieve low power operation. Table-1 shows comparison of various architecture-Flash, Folding & Interpolating and this design for medium resolution. It clearly indicates reduction in number of comparators due to the implemented design.

Table-1 Number Of Comparators Required By Various Adcs

Converter Resolution=N	Flash $(2^N - 1)$	Traditional F & I ADC	This design
5	31	11 (FF=4)	9 (FF=4)
6	63	19 (FF=4)/ 15 (FF=8)	17 (FF=4)/ 10 (FF=8)
7	127	23 (FF=8)	18 (FF=8)
8	255	39 (FF=8)	34 (FF=8)

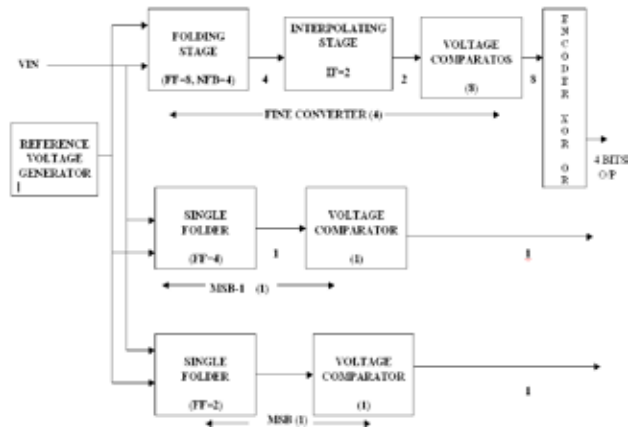


Fig. 2 : Block diagram of 6-bit folding & interpolating Analog to Digital Converter

IV. Design of Folding Amplifier

The function of a folder is to separate the input signal range into several intervals. The output signal, either in form of voltage signal or in form of current signal, of the folder is called a folding signal (FS). This section discusses proposed folding amplifier.

The goal of the folding amplifier is to overcome all the limitations of existing design, utilization of all transistor and minimizing power and settling time. In case of folding amplifier, upper

3-dB frequency is given by $f_{OUT} = \frac{1}{2\pi R_L C_{OUT}}$, where

$R_L = \frac{1}{\lambda \cdot I_{ss}}$. So high bias current is required in order to meet specified bandwidth. But increasing bias current required more power. In the design, large transistors helps in reducing mismatch errors such as offset as

$$V_{OS} = V_{TH1} + \sqrt{2I_{D1} \frac{L1}{W1}} - V_{TH2} + \sqrt{2I_{D2} \frac{L2}{W2}}$$

In this design, transistor sizes are kept minimum to reduce the capacitance, which ultimately reduces gain. So large value of load resistance is required to achieve high gain, which reduces bandwidth. This clearly indicates gain-bandwidth trade-offs.

The design uses stack of transistors to decrease C_{OUT} . Further transistor sizes are kept minimum and sufficient to reduce capacitance and still maintain the gain.

The first design of low voltage, low power folding amplifier is implemented for folding factor=4. The design consists of stack of differential pairs, reference voltage sources and single tail current source. Fig. 3 shows design of proposed folding amplifier. The first stage consists of a single differential pair while all other stages require two differential pairs. Single tail current source I_{tail} is shared between all differential pairs. Gate of transistor M1, M3, M5, M7, M9, M11 and M13 are connected to input V_{in} . V_{ref1} is applied to gate of M2, while V_{ref2} is connected to inputs of M4 & M6. Similarly V_{ref3} and V_{ref4} are applied to gate inputs of M8-M10 and M12-M14 respectively. The size of all the transistors of differential pairs is equal and kept minimum. Various zero crossing points are obtained when input V_{in} crosses reference voltage V_{ref} . The current flows through the transistors for all possibilities are shown below:

1. $V_{in} < V_{ref1}$ —M2-M6-M8-M14-L
2. $V_{in} > V_{ref1}$ —M1-M4-M10-M12-R

3. $V_{in} > V_{ref2}$ —M1-M3-M8-M14-L
4. $V_{in} > V_{ref3}$ —M1-M3-M7-M12-R
5. $V_{in} > V_{ref4}$ —M1-M3-M7-M11-L

The folding amplifier is designed with active pMOS load M16-M18. Cross-coupled pMOS load can be used to replace conventional resistor load because the value of resistance is not accurate in a CMOS process, which results in a big deviation of the output voltage. The active load works as an infinite load for differential mode signals and as a low-resistive load for common mode signals. Transistor M19 is used for equalization to reduce settling time. This also helps in reducing glitches [8]. The width of transistors M15-M18 (Active Load) and M19 (Equalization Switch) are kept higher compared to transistors M1-M14. Fig. 4 shows transient response indicating switching power and settling time of the folding amplifier.

In Fig. 3, there is no role of M5, M9 and M13 and so can be easily removed. Fig. 5 shows another implemented design, which utilizes all 14 transistors. The disadvantage of the design is it requires n+1 number of transistors at nth stage. This increases peak switching power and some of the transistors are utilized only once. However, due to different path of the current, settling time is less. The current flow for all the possibilities is shown below. The design can easily remove M12 transistor and drain of M7 can be connected to M14.

1. $V_{in} < V_{ref1}$ —M2-M5-M9-M14-L
2. $V_{in} > V_{ref1}$ —M1-M4-M8-M13-R
3. $V_{in} > V_{ref2}$ —M1-M3-M7-M12-L
4. $V_{in} > V_{ref3}$ —M1-M3-M6-M11-R
5. $V_{in} > V_{ref4}$ —M1-M3-M6-M10-L

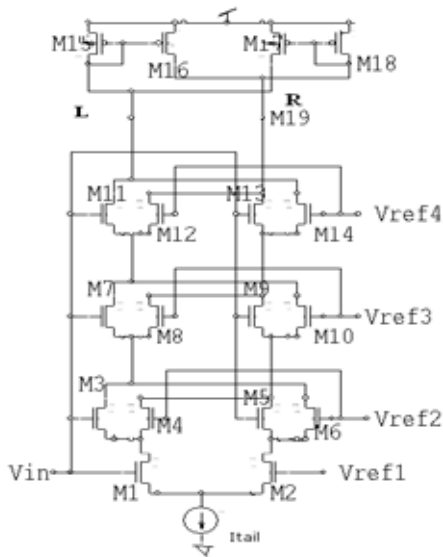


Fig.3 : Design-1 Low Voltage, Low Power Folding Amplifier with Folding Factor=4

Fig. 6 shows design with 12 transistors. The design utilizes all transistors and current flow is shown below.

1. $V_{in} < V_{ref1}$ —M2-M5-M7-M11-L
2. $V_{in} > V_{ref1}$ —M1-M4-M8-M12-R
3. $V_{in} > V_{ref2}$ —M1-M3-M7-M11-L
4. $V_{in} > V_{ref3}$ —M1-M3-M6-M10-R
5. $V_{in} > V_{ref4}$ —M1-M3-M6-M9-L

There are many advantages of the design. Due to single current source, static power consumption is minimum and no current source matching is required. Due to vertical stack of transistors, output capacitance is less, which reduces settling time and power. Also parasitic capacitance increases less rapidly with

increase in folding factor, compared to conventional voltage mode folding amplifier. However, as transistors are stacked vertically, available headroom decreases.

Table-1 shows comparison of all the three implemented designs and conventional design for folding factor=4. Lowering the supply voltage in folding circuit with source-coupled pairs prevents it from working because the conventional circuit has large output voltage range, and it is difficult to decrease the reference voltages. This is because decreasing reference voltages cause increasing zero-crossing error and decreasing peak output current [16]. However, careful design can overcome this limitation. The peak current can be given by (2).

$$I_p = I_s \left(\frac{\Delta V_{ref}}{\Delta V} \right) \sqrt{2 - \frac{1}{4} \left(\frac{\Delta V_{ref}}{\Delta V} \right)^2} - I_s \dots (2)$$

and

$$\Delta V_{ref} = V_{refN} - V_{refN-1} \quad (2 \leq N \leq 9),$$

$$\Delta V = \sqrt{\frac{2I_s}{\mu C_{ox} \frac{W}{L}}} = \frac{\sqrt{2I_s}}{G_m}$$

It can be observed that peak current decreases with

reduction in $\frac{\Delta V_{ref}}{\Delta V}$. The ratio $\frac{\Delta V_{ref}}{\Delta V}$ becomes lower with reduction in supply voltage. Accordingly peak current would decrease. However, this will not affect performance of ADC until there is no error in zero crossing point detection as decision is taken only at zero crossing points. Zero-crossing error is a difference between the zero crossing voltage at node N obtained from response and actual

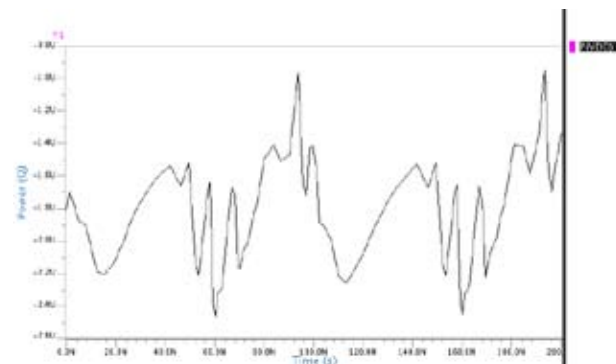
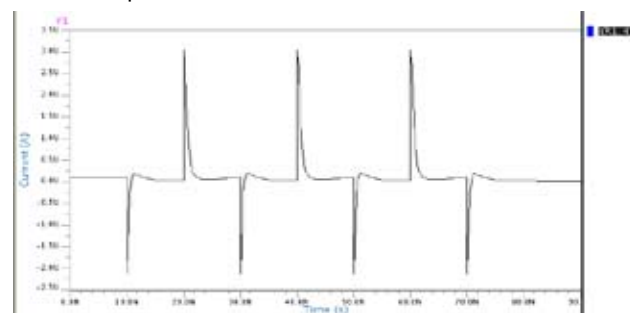


Fig.4: (a) Switching Power of Folding Amplifier for Sine Input



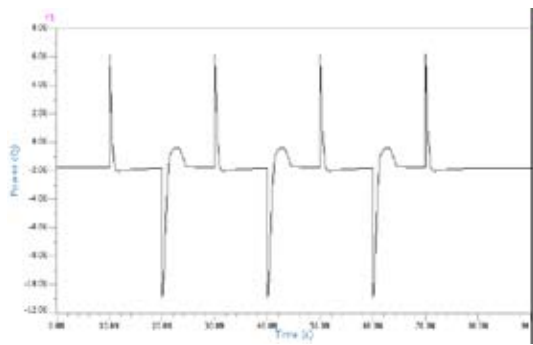


Fig.4: (b) Switching Power and Current for Pulse input reference voltage at node N. To avoid zero

crossing point error ΔV_{ref} should be higher than ΔV . For this

design $\Delta V_{ref} = 0.2V > \Delta V = 0.12V$ and thus no zero crossing error.

Fig. 7 shows generated 32-zero crossing points with FF=8. The swing values are also shown in that. The maximum swing is 3.25V (approx. equal to supply voltage-drop)

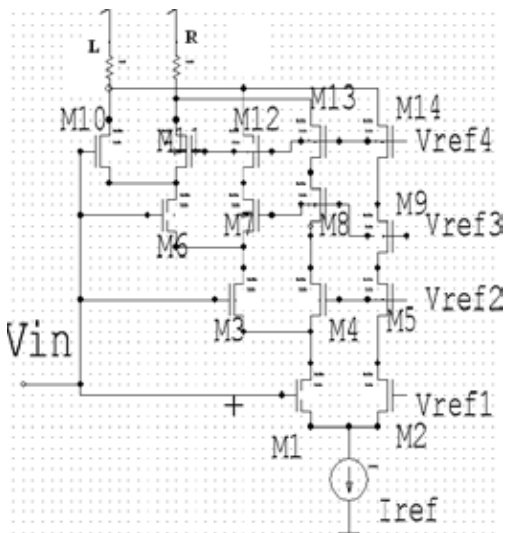


Fig.5: Design-2 Folding Amplifier with folding factor=4

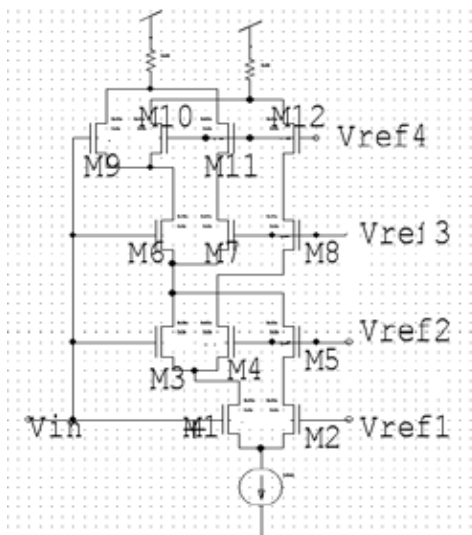


Fig.6: Design-3 Folding Amplifier with

folding factor=4

V. Interpolation Techniques

Interpolation is often employed to generate extra folding waveforms without increasing number of folding amplifiers. There are basically two methods to interpolate the folded signals, namely voltage-mode (resistive) interpolation and current-mode interpolation.

The current-mode interpolation is based on summation of currents reflected through current mirrors with different ratios.

Table-2 Performance Comparison of Folding Amplifiers

Parameters	Conventional	Design -1	Design -2	Design -3
Technology	0.18 μ m	0.18 μ m	0.18 μ m	0.18 μ m
Folding Factor	4	4	4	4
Ref. Current sources	4	1	1	1
Static Power	6.4 μ W	1.7 μ W	1.7 μ W	1.7 μ W
Switching Power-peaks-sine wave	6.8 μ W-7.6 μ W	1.3 μ W-2.3 μ W	0.85 μ W-2.25 μ W	1.4 μ W-2.2 μ W
Switching Power peak range at 50MHz pulse	16 μ W	12 μ W	10 μ W	11 μ W
Settling Time	0.8ns	0.413 ns	0.342 ns	0.38 ns

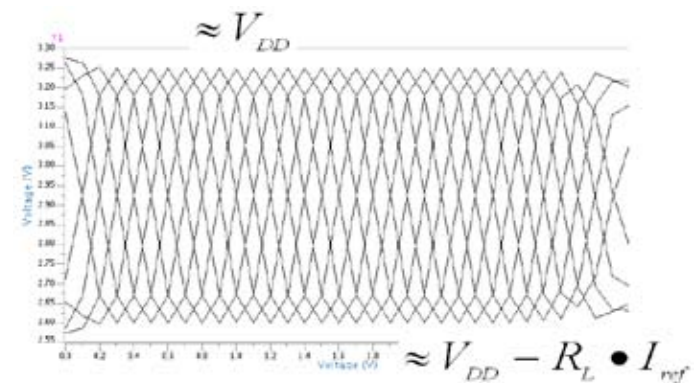


Fig. 7: Generated 32- Zero Crossing points

However this method is complex proves to be power hungry and not very precise due to the non-idealities of the current mirrors [13, 14].

The voltage-mode (resistive) interpolation can be implemented using a resistance ladder. The advantage of a voltage-mode interpolation is its design simplicity and low power operation. Fig. 8 shows zero crossing points generated with folding and interpolating stage.

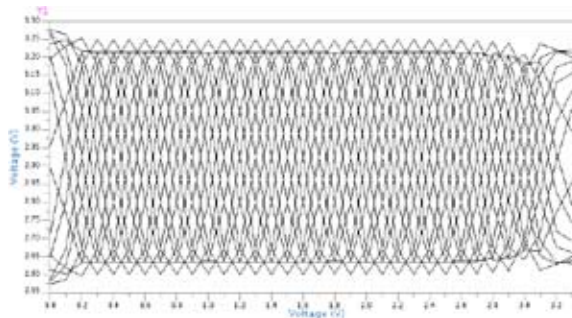


Fig.8 : Generated 64-zero crossings using folding & interpolating

VI. Low Power Comparator

In order to achieve low power, high-speed operation of the design, comparator is another important block. When a comparator must drive a significant amount of output capacitance in very short times, it is advisable to follow the latch by circuits that can quickly generate large amount of current. A high-speed comparator following these principles is designed in [15]. The first stage is a low gain, high bandwidth preamplifier that drives a latch (Decision Circuit). The latch outputs are used to drive an inverter (Output Stage) as shown in Fig. 9.

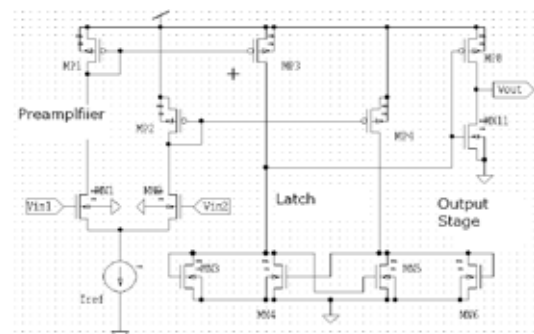


Fig.9 : Low Power Comparator

VIII. Simulation Results

The 6-bit folding & interpolating converter is simulated at 0.35 μ m technology, 3.3V supply voltage. Instead of using traditional flash architecture for implementing coarse converter, folding circuit is used as pre-processing. The implemented coarse converter is shown in fig 10(a) and fig. 10 (b) shows coarse converter bits. Folding amplifier and comparators are designed using low power approach. The simulation result of the fine converter- cyclic thermometer code is shown in fig. 11. The cyclic output can be easily converted into binary code. The advantage of the architecture is it requires only 10 comparators at the cost of folding amplifiers. The folding amplifiers used in coarse converter help in reducing latency difference of fine and coarse converter. To convert cyclic code into binary, logic shown in equations (1) can be used, comparing binary and cyclic code. The encoder based on XOR-OR logic can be used to convert the cyclic code into binary. The total power required is only 12.45mW.

Encoder logic:

$$B3 = C7$$

$$B2 = C7 \oplus C3$$

$$B1 = C7 \oplus C5 \oplus C3 \oplus C1$$

$$B0 = C7 \oplus C6 \oplus C5 \oplus C4 \oplus C3 \oplus C2 \oplus C1 \oplus C0 \dots (3)$$

Where B0 to B3 are 4-bit fine converter output & C0 to C7 are 8-bit fine comparator output.

The coarse converter divides input into several intervals and provides MSBs. In most of the design, coarse converter is

similar to Flash. In this design, folding amplifier is used to generate MSBs. This helps in reducing number of comparators and encoder logic.

VIII. Conclusions

In this paper, low power folding and interpolating ADC is designed with minimum comparators and hardware. The architecture uses folding pre-processing circuit for both coarse & fine converter. To achieve low power operation, folding block, comparator & encoder are optimized. The design is simulated using 0.35 μ m technology at 3.3V. The paper also compares the architecture with existing one, to show the reduction in number of comparators. The simulation results indicate that the design achieves low power operation. Due to cyclic output of folding block comparison, number of comparators required is only 10 in case of 6-bit converter. The design also helps in reducing latency difference of coarse and fine converter.

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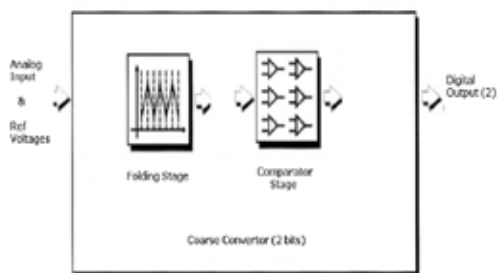


Fig. 10 (a) : Coarse Converter

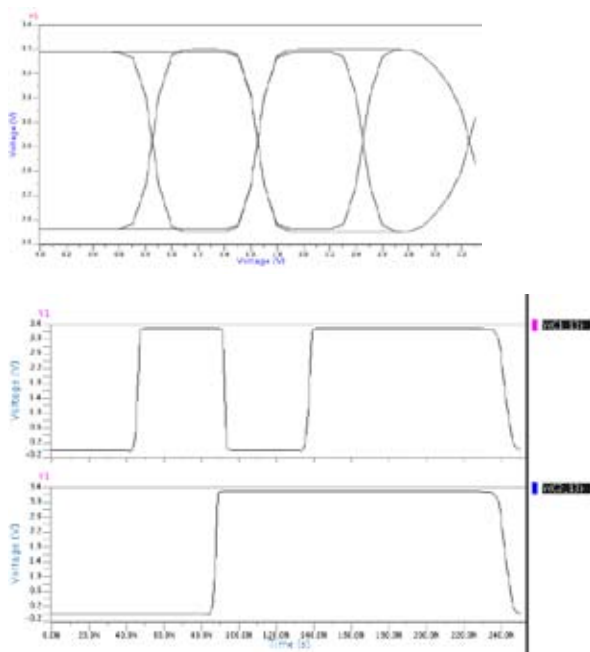


Fig. 10 (b) : Coarse bits

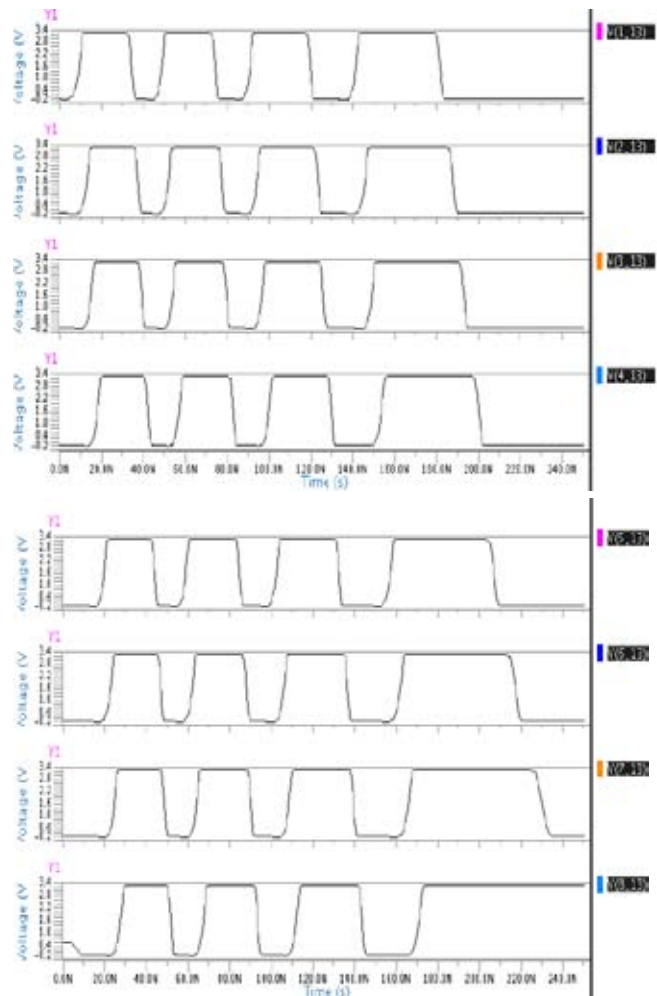


Fig. 11 : Cyclic Thermometer Code of Fine Converter-Four bits

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